

SNE2302 300mA, Low Power, Low Dropout, RF Linear Regulators

Features

- Low Dropout Voltage
- Thermal Overload Protection
- Built-In Fold Back Protection Circuit
- 20 μ A Low Ground Current
- 10nA Logic-Controlled Shut down
- 1.6V to 5.5V Input Voltage Range
- Fixed Outputs 0.8V to 5.0V
- Short Auto-Discharge Function
- 300mA Output Current
- High Output Voltage Accuracy
- Quick Start-Up Time
- -40°C to +125°C Operating Temperature Range
- Available in Green UTDFN-1 \times 1-4L and SOT-23-5 Packages

Applications

- Cellular Telephones
- PCMCIA Cards
- Modems
- Hand-Held Instruments
- Palmtop Computers
- Portable/Battery-Powered Equipment

General Description

The SNE2302 series low-power, low-dropout, CMOS linear voltage regulators operate from a 1.6V to 5.5V input voltage and deliver up to 300mA output current. They are the perfect choice for low voltage, low power applications. A low ground current makes this part attractive for battery operated power systems. The SNE2302 series also offer low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the SNE2302 series' low output noise and high PSRR.


Other features include a 10nA logic-controlled shutdown mode, short current limit and thermal shutdown protection.

The SNE2302 has auto-discharge function to quickly discharge V_{OUT} in the disable status.

The SNE2302 is available in Green UTDFN-1 \times 1-4L SOT-23-5 and packages. It operates over an ambient temperature range of -40°C to +125°C.

Ordering Information

Part Number	V_{OUT} (V)	Accuracy	Temperature	Package	Ordering Number	Packing Option
SNE2302	XX	2.5%	-40~+125°C	SOT-23-5	SNE2302-XXHAREA1R	Tape and Real, 3000
SNE2302	XX	2.5%	-40~+125°C	UTDFN-1 \times 1-4L	SNE2302-XXHARHC1R	Tape and Real, 10000

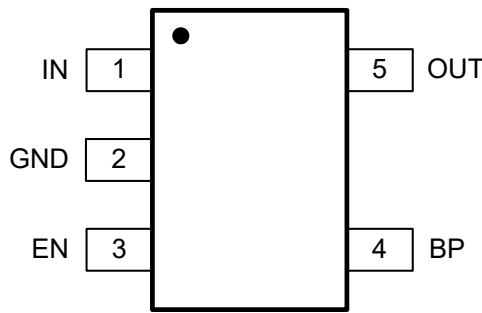
 **Note:** XX indicates 0.8V~5.0V. For example, 33 means product outputs 3.3V.

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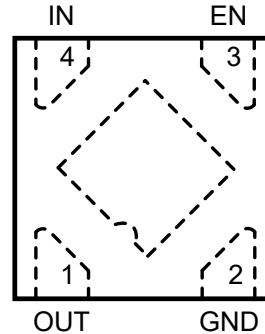
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1 Pin Description

1.1 Pin Assignment



SOT-23-5 (Top View)



UTDFN-1x1-4L (Top View)

1.2 Pin Definition

Pin		Name	Function
UTDFN-1x1-4L	SOT-23-5		
1	5	OUT	Regulator Output.
2	2	GND	Ground.
3	3	EN	Enable Pin. This pin has an internal pull-down resistor. A logic low reduces the supply current to less than 1μA. Connect to IN for normal operation.
4	1	IN	Regulator Input. Supply voltage can range from 1.6V to 5.5V. Bypass with a 1μF capacitor to GND.
	4	BP	Reference-Noise Bypass Pin . Bypass with a low-leakage 0.01μF ceramic capacitor for reduced noise at the output. The capacitor is recommended to be placed very close to the pin for high PSRR.
Exposed Pad			The exposed pad should be connected to a large ground plane to maximize thermal performance.

2 Specifications

2.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	
IN to GND	V_{IN}	-0.3 ~ 6	V	
EN to GND	V_{EN}	-0.3 ~ 6	V	
OUT, BP to GND	V_{OUT}	-0.3 ~ ($V_{IN}+0.3$)	V	
Power Dissipation @ $T_A = 25^\circ\text{C}$	UTDFN-1×1-4L	$P_{D, UTDFN-1\times 1-4L}$	400	mW
	SOT-23-5	$P_{D, SOT-23-5}$	390	mW
Package Thermal Resistance	UTDFN-1×1-4L	$\theta_{JA, UTDFN-1\times 1-4L}$	280	$^\circ\text{C/W}$
	SOT-23-5	$\theta_{JA, SOT-23-5}$	285	$^\circ\text{C/W}$
Operating Temperature Range	T_A	-40 ~ +125	$^\circ\text{C}$	
Junction Temperature	T_J	150	$^\circ\text{C}$	
Storage Temperature Range	T_{STG}	-65 ~ 150	$^\circ\text{C}$	
Lead Temperature (Soldering, 10s)	T_{SOLDER}	260	$^\circ\text{C}$	
ESD Susceptibility	HBM	$V_{ESD, HBM}$	4000	V
	MM	$V_{ESD, MM}$	400	V

Note: Stresses beyond those listed under “AbsoluteMaximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Attention: This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SENASIC recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SENASIC reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SENASIC sales office to get the latest datasheet.


2.2 Electrical Characteristics

$V_{IN} = V_{OUT(NOMINAL)} + 0.5\text{V}$ or 2.5V , whichever is greater, Full = -40°C to $+125^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit
Input Voltage	V_{IN}		$+25^\circ\text{C}$	1.6		5.5	V
Output Voltage Accuracy		$I_{OUT} = 0.1\text{mA}$	$+25^\circ\text{C}$	-2.5		+2.5	%

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit	
Maximum Output Current ^[1]			+25°C	300			mA	
Current Limit	I_{LIM}		+25°C	360	560		mA	
Supply Pin Current	I_Q	No Load, $V_{EN} = V_{IN}$	+25°C		20	26	μA	
Dropout Voltage ^[2]	V_{DROP}	$I_{OUT}=300mA$	$V_{OUT}=0.8V$	+25°C		940	1200	mV
			$V_{OUT}=0.9V$	+25°C		840	1100	
			$1.0V \leq V_{OUT} < 1.1V$	+25°C		780	1000	
			$1.1V \leq V_{OUT} < 1.2V$	+25°C		680	900	
			$1.2V \leq V_{OUT} < 1.5V$	+25°C		590	800	
			$1.5V \leq V_{OUT} < 1.8V$	+25°C		420	550	
			$1.8V \leq V_{OUT} < 2.1V$	+25°C		320	420	
			$2.1V \leq V_{OUT} < 2.5V$	+25°C		260	340	
			$2.5V \leq V_{OUT} < 3.0V$	+25°C		215	280	
			$3.0V \leq V_{OUT} < 3.6V$	+25°C		190	250	
$3.6V \leq V_{OUT} \leq 5.0V$	+25°C		165	210				
Line Regulation		$V_{IN}=1.6V$ or $(V_{OUT}+0.5V)$ to 5.5V, $I_{OUT}=1mA$	$1.8V \leq V_{OUT} \leq 3.3V$	+25°C		0.01	0.06	%V
			$V_{OUT} < 1.8V$, $V_{OUT} > 3.3V$	+25°C		0.01	0.1	
Load Regulation	ΔV_{OUT}	$I_{OUT} = 0.1mA$ to 300mA	+25°C		12	40	mV	
Short Current Limit	I_{SHORT}	$V_{OUT} = 0V$	+25°C		200		mA	
Power Supply Rejection Ratio	PSRR	$C_{BP}=0\mu F$, $I_{OUT}=30mA$, $C_{OUT}=1\mu F$, $V_{IN}=V_{OUT}+1V$, $\Delta V_{RIPPLE} = 0.2V_{P-P}$	$f = 217Hz$	+25°C		80		dB
			$f = 1kHz$	+25°C		75		
			$f = 217Hz$	+25°C		82		
			$f = 1kHz$	+25°C		70		
Output Voltage Noise	e_n	$C_{BP}=0\mu F$, $f = 10Hz$ to 100kHz, $C_{OUT}= 1\mu F$, $V_{OUT}=1.8V$	$I_{OUT}=0mA$	+25°C		100		μV_{RMS}
			$I_{OUT}=30mA$	+25°C		200		
			$I_{OUT}=0mA$	+25°C		30		
			$I_{OUT}=30mA$	+25°C		75		
SHUTDOWN								
EN Input Threshold	V_{IH}	$V_{IN} = 1.6V$ to 5.5V	Full	1.5			V	
	V_{IL}		Full			0.4		
EN Input Bias Current	I_{BH}	$V_{EN} = 5.5V$	Full		0.8	2	μA	
	I_{BL}	$V_{EN} = 0V$	Full		0.01	1		
Shut down Supply Current	$I_Q (SHDN)$	$V_{EN} = 0V$	Full		0.01	1	μA	

Parameter	Symbol	Conditions	Temp	Min	Typ	Max	Unit
Start-Up Time ^[3]	t _{STR}	C _{OUT} = 1μF, No Load	+25°C		30		μs
R _{ON} of Discharge MOSFET		V _{IN} = 4.0V, V _{EN} = 0V	+25°C		50		Ω
THERMAL PROTECTION							
Thermal Shutdown Temperature	T _{SHDN}				140		°C
Thermal Shutdown Hysteresis	ΔT _{SHDN}				15		°C

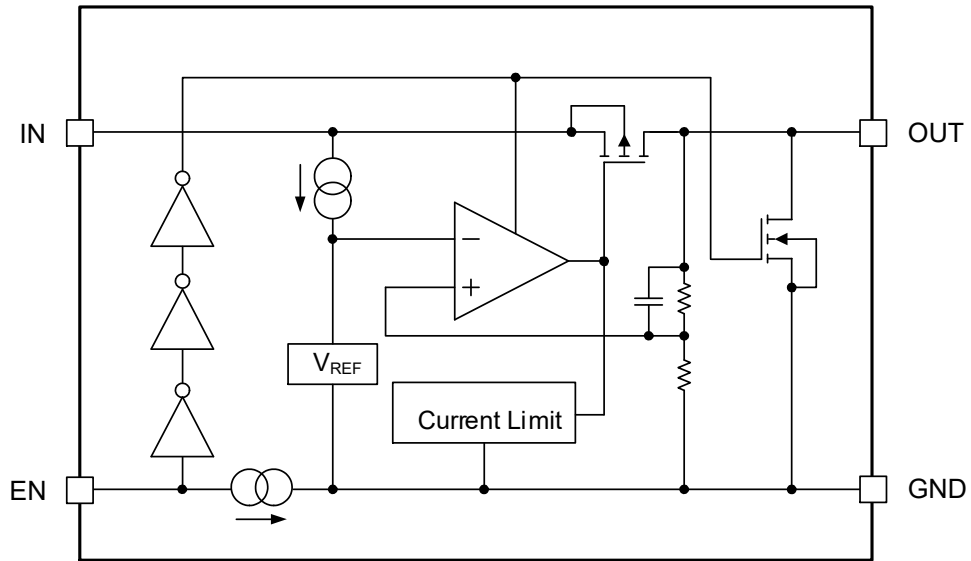
 **Note:**

[1] Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when $V_{IN} < V_{OUT} + V_{DROP}$.

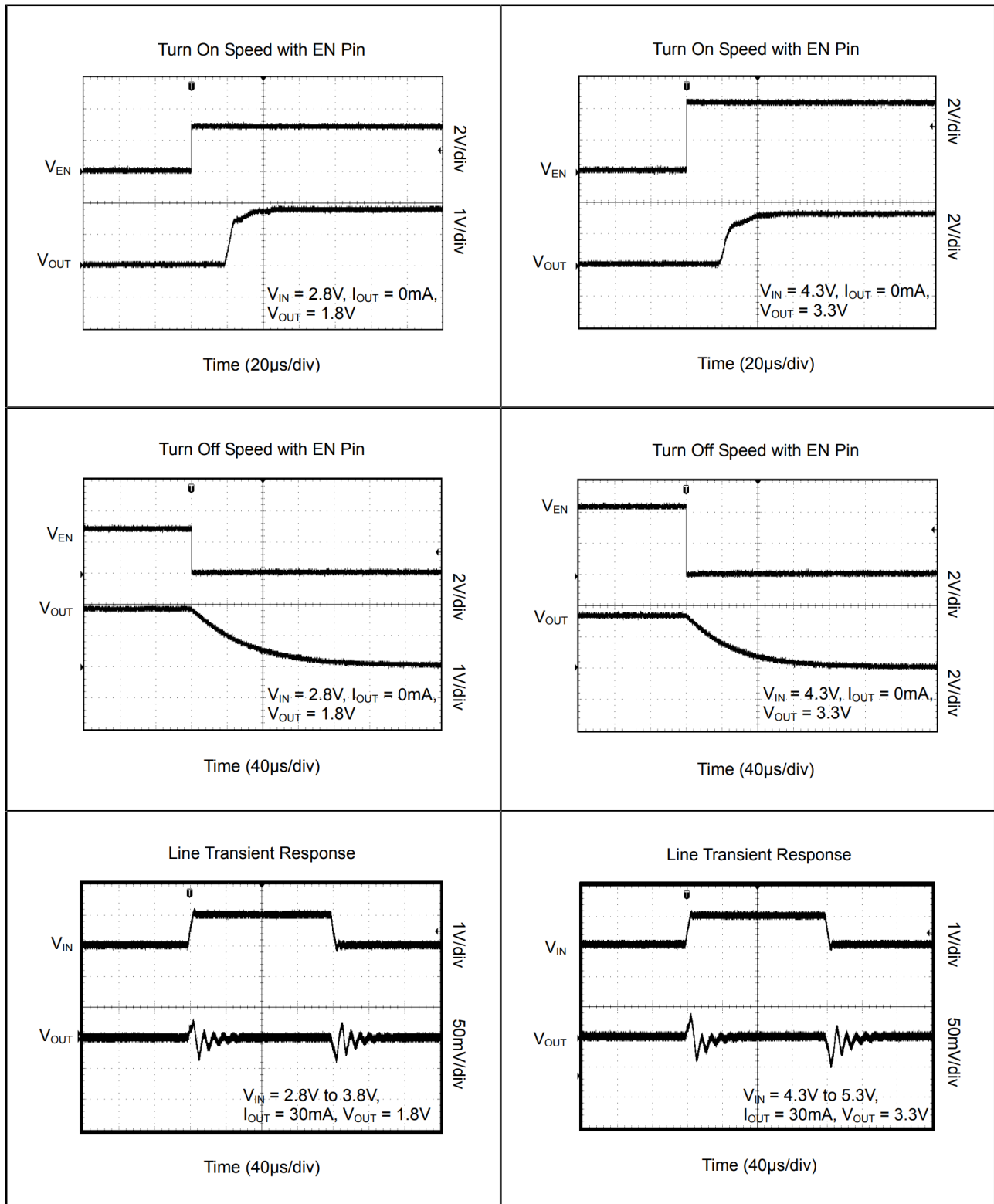
[2] The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 100mV below the value of V_{OUT} for $V_{IN} = V_{OUT} + 0.5V$ or 2.5V.

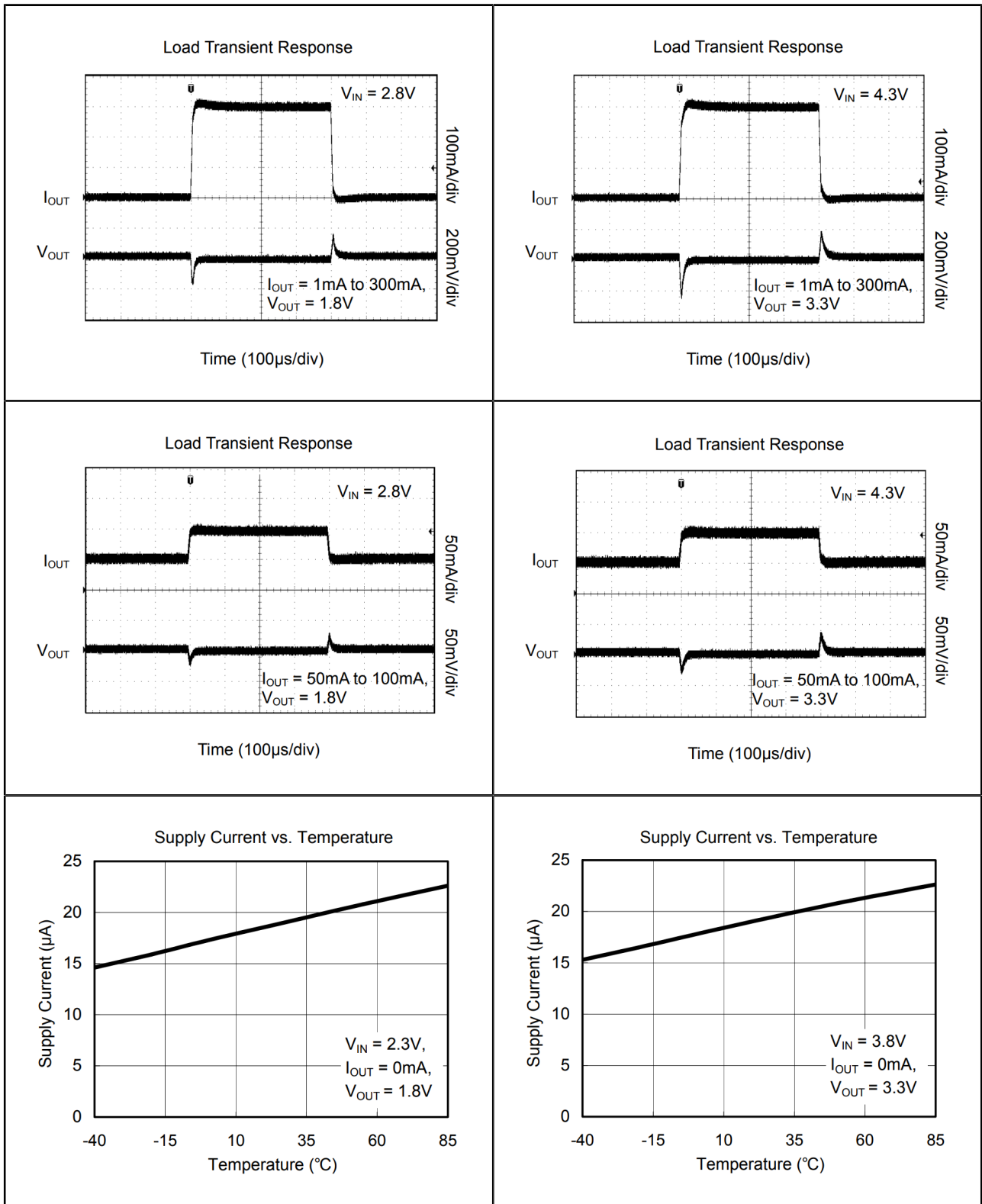
[3] Time needed for V_{OUT} to reach 90% of final value.

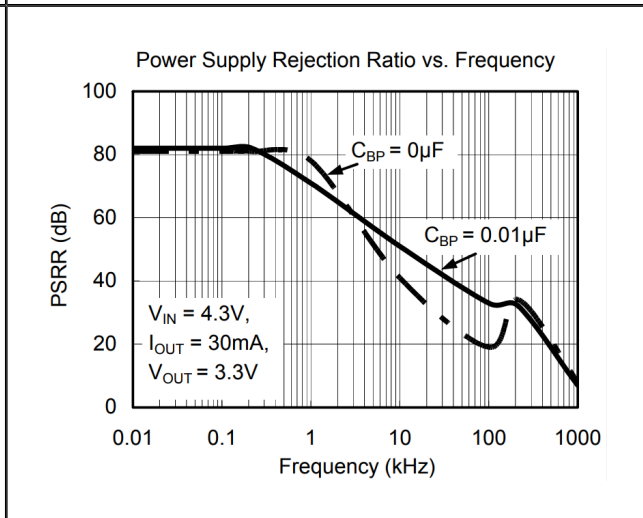
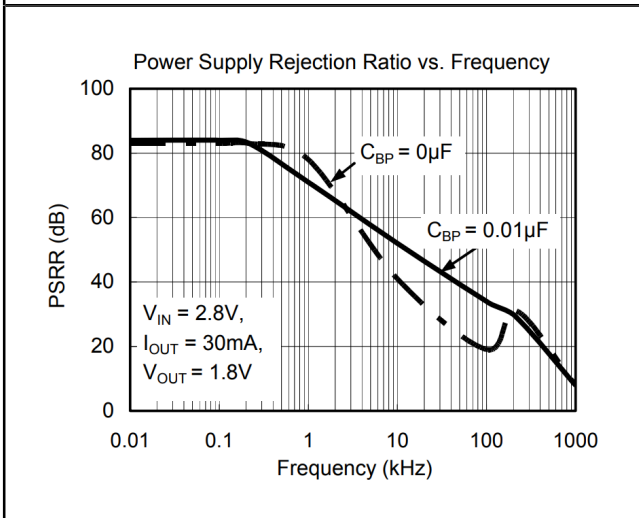
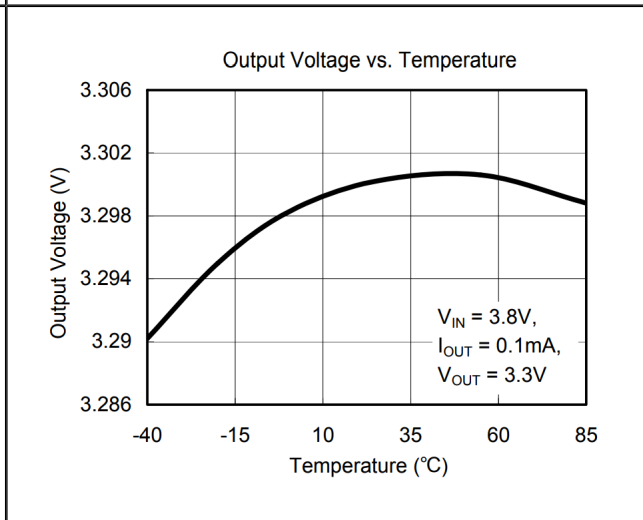
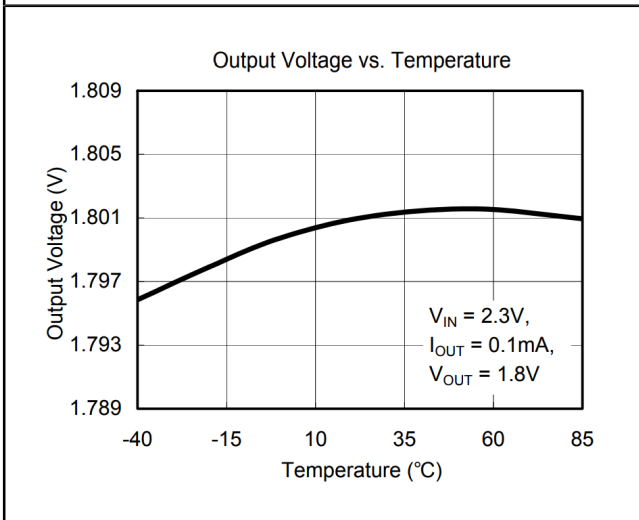
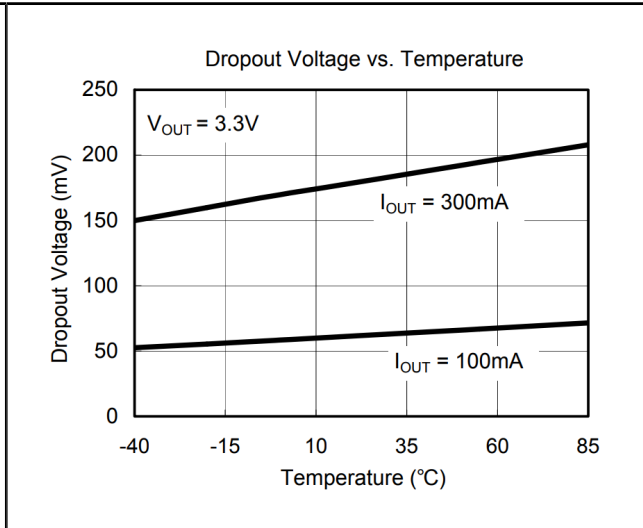
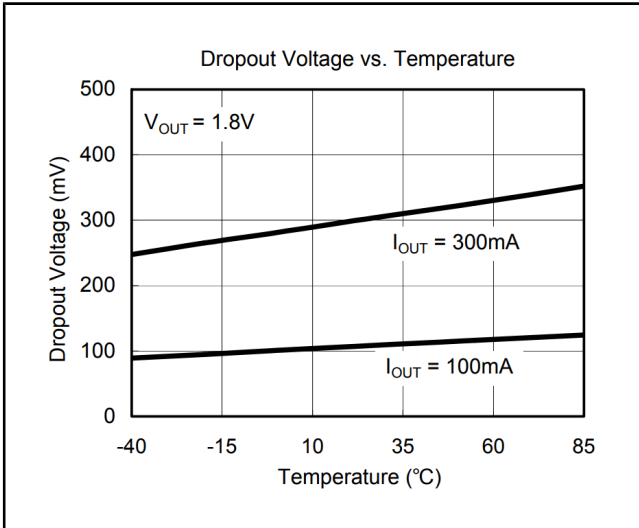
3 Simplified Block Diagram

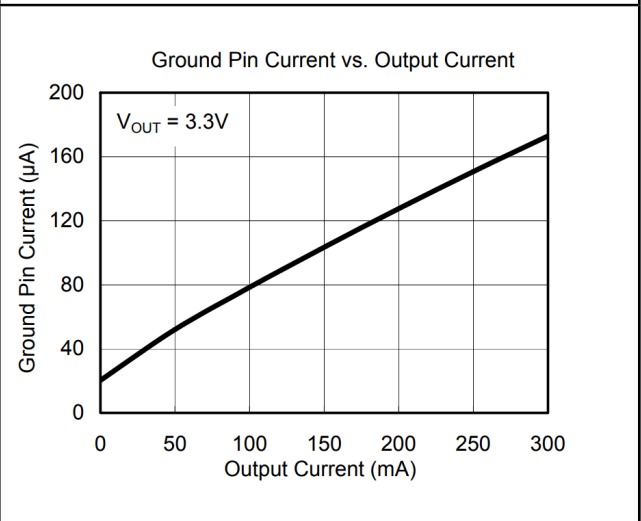
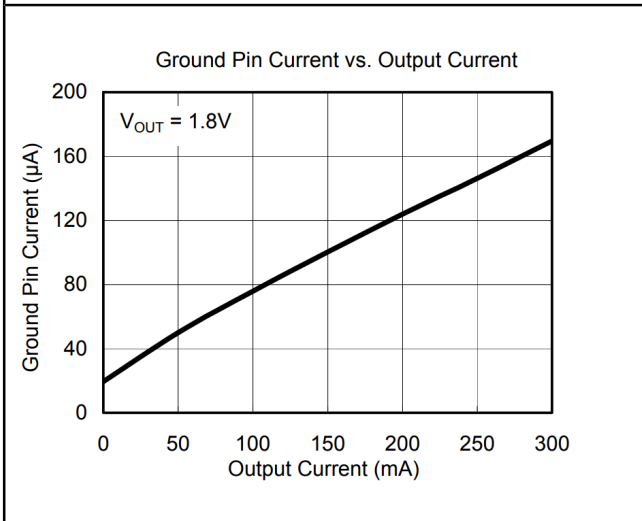
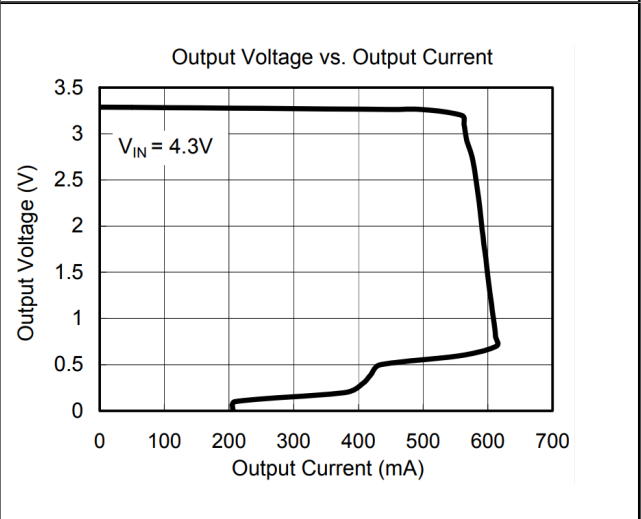
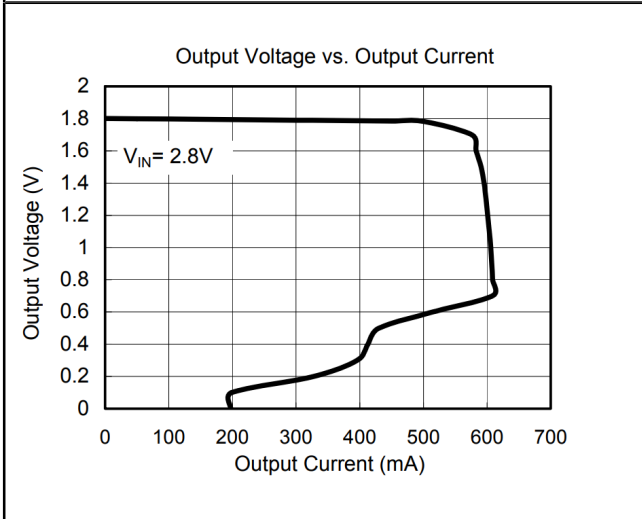
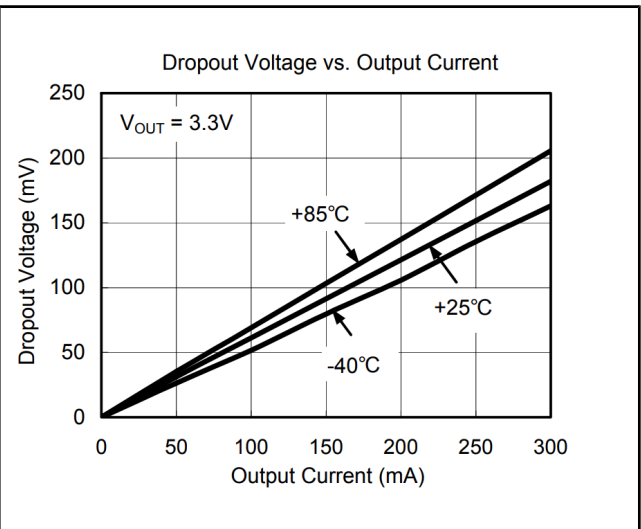
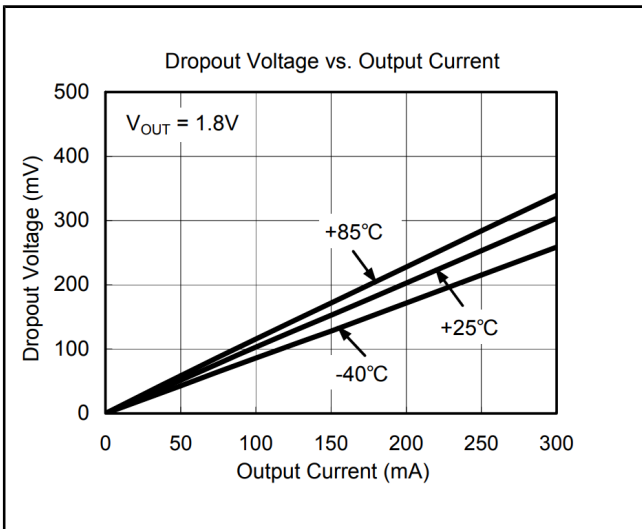


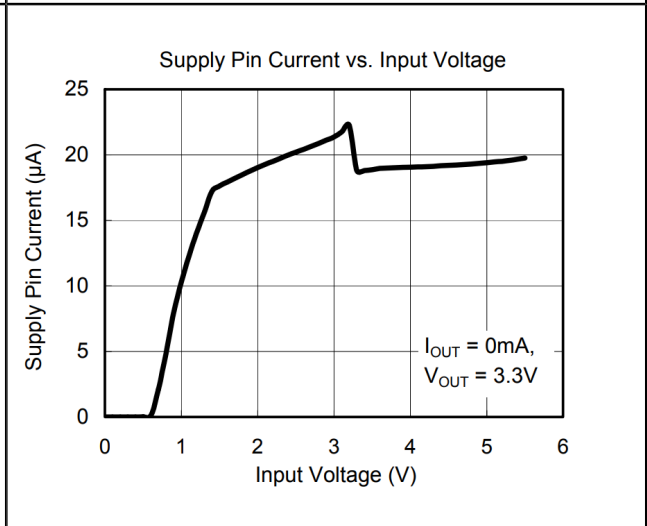
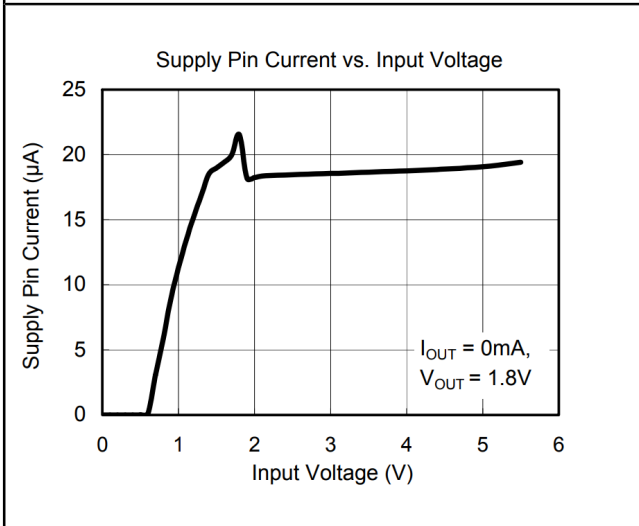
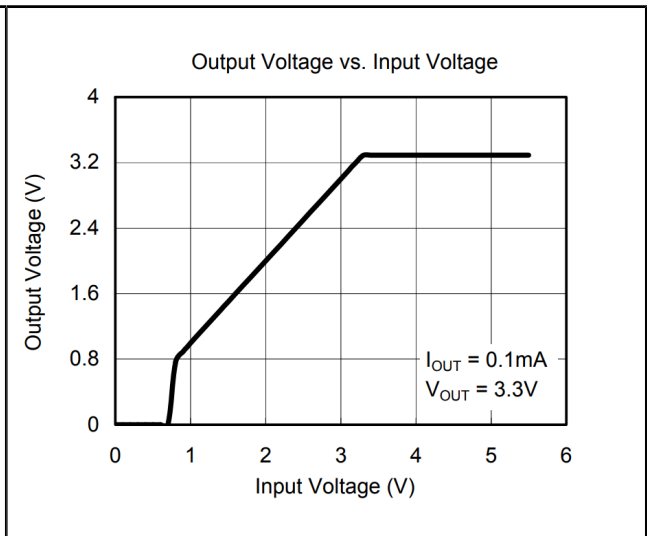
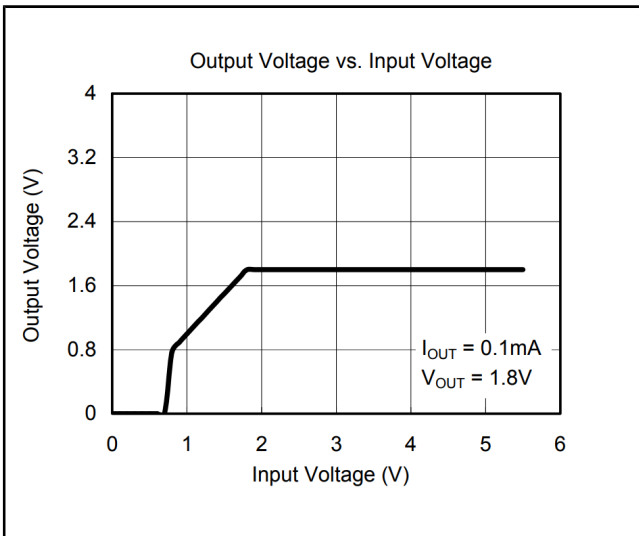
4 Performance Characteristics











5 Typical Application Circuit

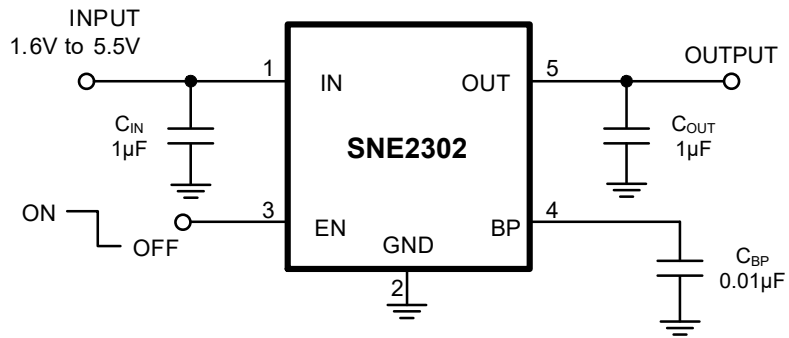


Figure 5-1 Typical Application Circuit (SOT-23-5)

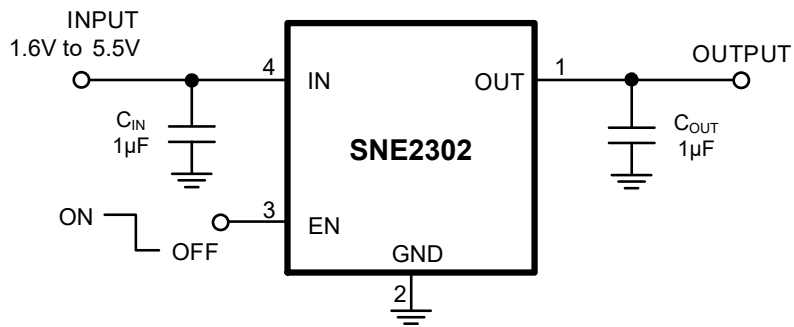


Figure 5-2 Typical Application Circuit (UTDFN-1x1-4L)

6 Application Note

When LDO is used in handheld products, attention must be paid to voltage spikes which could damage SNE2302. In such applications, voltage spikes will be generated at charger interface and V_{BUS} pin of USB interface when charger adapters and USB equipments are hot-plugged. Besides this, handheld products will be tested on the production line without battery. Test engineer will apply power from the connector pin which connects with positive pole of the battery. When external power supply is turned on suddenly, the voltage spikes will be generated at the battery connector. The voltage spikes will be very high, and it always exceeds the absolute maximum input voltage (6.0V) of LDO. In order to get robust design, design engineer needs to clear up this voltage spike. Zener diode is a cheap and effective solution to eliminate such voltage spike. For example, BZM55B5V6 is a 5.6V small package Zener diode which can be used to remove voltage spikes in cell phone designs. The schematic is shown below.

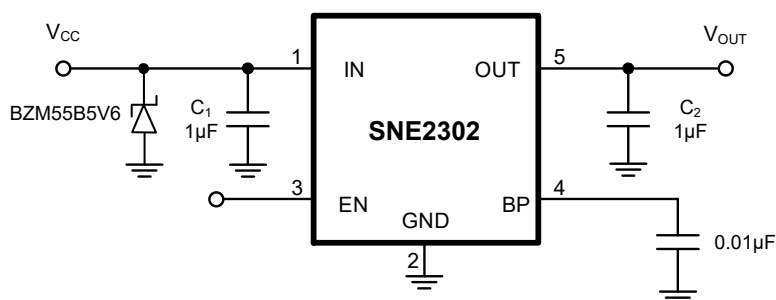


Figure 6-1 Handheld product application circuit (SOT-23-5)

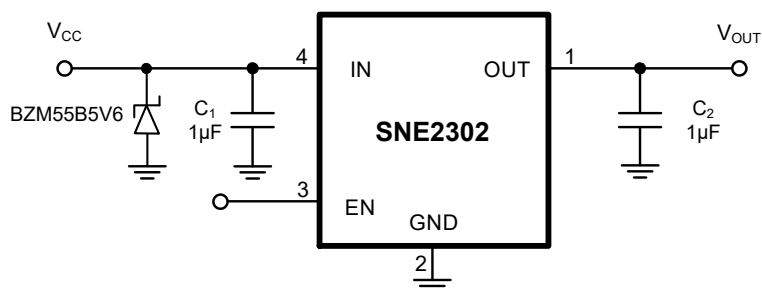
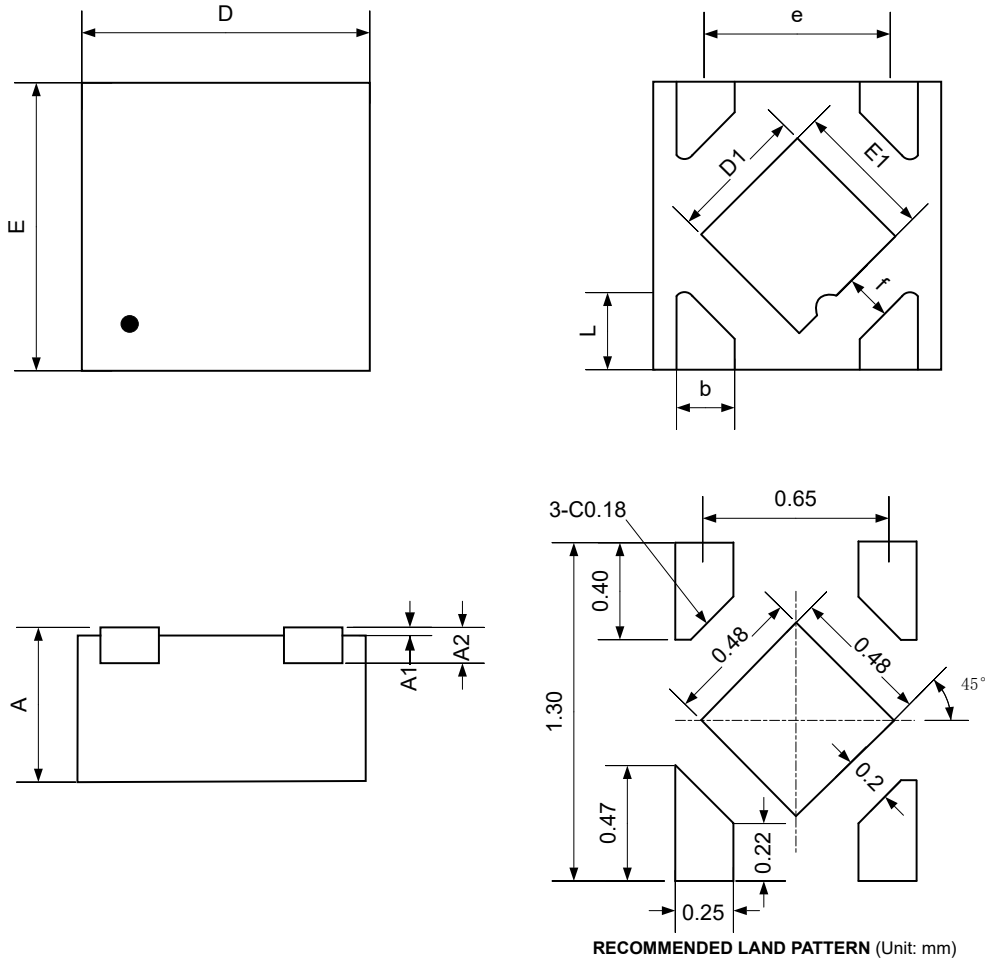


Figure 6-2 Handheld product application circuit (UTDFN-1x1-4L)

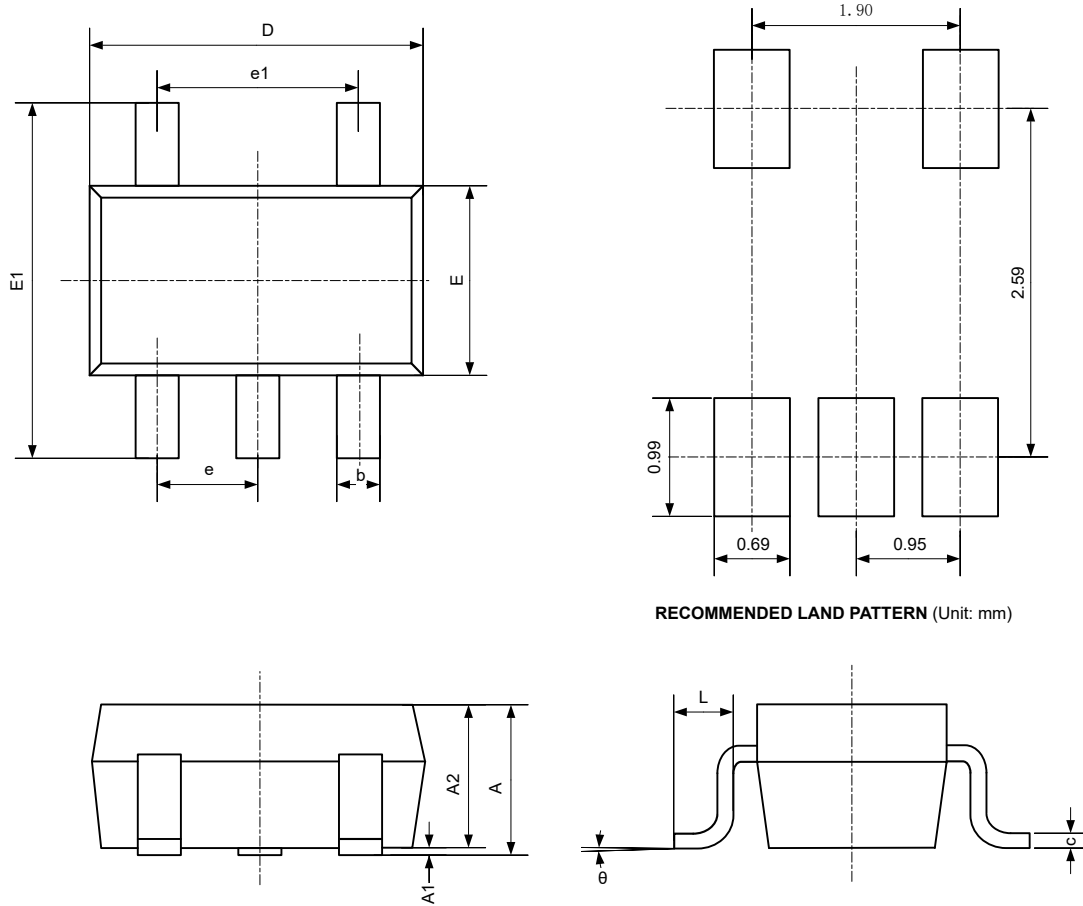
7 Package Outline

7.1 UTDFN-1x1-4L



Symbol	Dimensions in Millimeters		
	Min	Nominal	Max
A	0.500	0.550	0.600
A1	0.000		0.050
A2	0.152 REF		
D	0.950	1.000	1.050
D1	0.450	0.500	0.550
E	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.175	0.225	0.275
e	0.625 BSC		
f	0.195 REF		
L	0.200	0.250	0.300

7.2 SOT-23-5



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

8 Revision History

Version	Date	Description
0.1	2022/07/12	Initial release

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