SNP739D51

Highly integrated tire pressure monitoring sensor

SNP739D51 Datasheet

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Consultation Information

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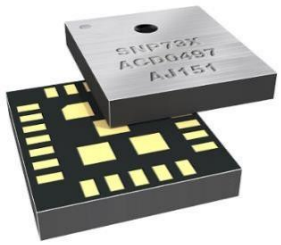
Feature

- Calibrated pressure sensor for absolute pressure measurement with optional measurement range:900kPa
- Temperature and supply voltage sensors
- 12-bit analog-to-digital converter (ADC12) with two external I/O inputs
- **RF Transmitter**
  - On chip PA
  - 315/433MHz supported
  - Support ASK/FSK modulation
  - Support Manchester/PWM/Bi-Phase/ Mark-space encoding
- **LF Receiver**
  - Support LF programming
  - 3.9kbps supported
  - Manchester encoding
- **On chip RC oscillator**
  - 1kHz/39kHz/2MHz
- **MCU**
  - 8-bit MCU
  - Based on 1T 8051 core
  - 16K Bytes Flash
  - 32K Bytes ROM
  - 256 Bytes data RAM and 128 Bytes retention RAM
  - 6 GPIOs, All GPIOs support low power wakeup
  - SPI/UART/I2C/LIN interface supported
  - Timer 8 with PWM function
- Standby current 0.2μA
- Package: LGA 24pins. 6.0mmx5.0mmx1.9mm

Applications

- Tire Pressure Monitoring sensor
- MEMS sensing



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List of Abbreviations (keyword:TPMS)

Abbreviations	Full spelling
PA	Power Amplifier
AON	Always Online
LGA	Land Grid Array
WAM	Wheel Auto Mapping
MCU	Microcontroller Unit
FLASH	Flash Memory
ADC	Analog to Digital Converter
RAM	Random Access Memory
RF	Radio Frequency
LF	Low Frequency
UART	Universal Asynchronous Receiver/Transmitter
SPI	Serial Peripheral Interface
I2C	Inter Integrated Circuit
TPMS	Tire Pressure Monitoring System
MEMS	Micro Electromechanical System
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying
CRC	Cyclic Redundancy Check
POR	Power On Reset
BOR	Brown Out Reset
XTAL	External Crystal Oscillator
SFR	Special Function Register
IRAM	Internal RAM
XRAM	External RAM
PWM	Pulse Width Modulation
PLL	Phase Locked Loop
CPU	Central Processing Unit

1 Introduction

SNP739D consists of 16K Flash memory, 32K ROM memory, interrupt bus, configuration registers and control bus which operate the analogue circuitry all of which are controlled via an 8-bit integrated microcontroller.

Measurements of pressure, temperature, and battery voltage are performed under software control, allowing the application software to format and prepare the data for RF transmission.

A software defined wakeup mechanism is developed for minimizing power consumption. An Interval timer controls the timing of measurements and transmissions.

Embedded LF receiver can help SNP739D to wake up at regular intervals and it works independently with no CPU aids at any time of user definition timeout period, thus helps power saving greatly, The LF receiver supports wireless Flash programming to the chip without I2C communication which demonstrates high efficiency in customer firmware development phase. The integrated microcontroller's instruction set is compatible to the standard 8051 processor. It is equipped with hardware Manchester, bi-phase encoder/ decoder and CRC generator and checker, which enable easy implementations of customer specific applications.

The low-power RF Transmitter for 315 and 434 MHz contains a fully integrated PLL synthesizer, an ASK/FSK modulator and an efficient power amplifier.

On-chip Flash memory stores the customer specific application program code, the unique ID-number and the calibration data for the sensor. Additionally, the embedded library functions developed by SENASIC cover standard tasks used by the application.

Table 1-1 Order Information

Model	Pressure Range	Package	Packing Option
SNP739D51CLE	100 ~ 900	LGA24	3000ea/Reel

2 Pin Description

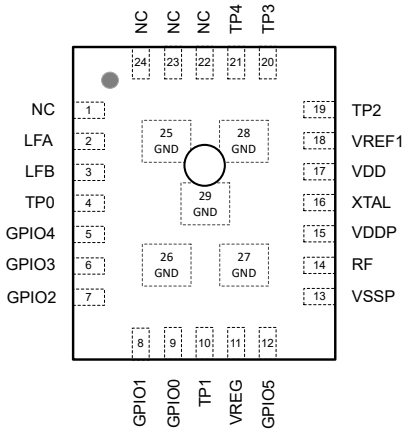


Figure 2-1 Pin Configuration(Top View)

Table 2-1 Pin Description

Pin No.	Name	Pin Type	Function
1	NC		Connect to GND
2	LFA	Analog IO	LF channel coil connection
3	LFB	Analog IO	LF channel coil connection
4	TP0		Connect to GND
5	GPIO4	Digital IO	GPIO/SPI MISO/UART RXD
6	GPIO3	Digital IO	GPIO/SPI MOSI/UART TXD
7	GPIO2	Digital IO	GPIO/SPI CSN
8	GPIO1	Digital IO	GPIO/I2C data
9	GPIO0	Digital IO	GPIO/I2C Clock
10	TP1		Connect to GND
11	VREG	Supply	Internal regulator,it must not be used as external current source.
12	GPIO5	Digital IO	GPIO/SPI CLK
13	VSSP	Supply	Ground
14	RF	Analog IO	RF output
15	VDDP	Supply	Battery supply 3V
16	XTAL	Analog IO	XTAL pin
17	VDD	Supply	Battery supply 3V
18	VREF1	Analog IO	100nF to ground
19	TP2		N.C., just place a test point on board
20	TP3		N.C., just place a test point on board
21	TP4		N.C., just place a test point on board
22	NC		Not connect
23	NC		Not connect
24	NC		Not connect
25~29	GND	Supply	Ground

3 Specification

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Max.Supply Voltage	V_{DDmax}	-0.3		+3.8	V	
ESD robustness HBM	V_{ESD_HBM}	-2000		+2000	V	All pins according to JS-001-2014
		-4000		+4000	V	RF pin according to JS-001-2014
ESD robustness CDM	V_{ESD_CDM}	-500		+500	V	All pins according to JS-002-2014
Latch up	I_{LU}	-100		+100	mA	All pins according to JEDEC 78D
Input Voltage	V_{in}	-0.3		V_{DD}+0.3	V	GPIO0~ GPIO5
		-0.3		V_{DD}+0.3	V	XTAL
		-0.3		V_{DD}+0.3	V	LFA, LFB
Dynamic voltage at RF pin	V_{dyn_PAOUT}			V_{DD} +0.3	V	
DC current	I_{DC}	-10		+10	mA	GPIO0~ GPIO5
		-10		+10	mA	XTAL
		-10		+10	mA	LFA, LFB
Input pressure	P_{in}	0		2000	kPa	
		2000		2500	kPa	Maximal 2s 5 times over lifetime
Constant Acceleration	a_{CA}			3500	g	Tested in +/- x,y,z- direction.(Device unpowered)
Mechanical Shock	a_{MS}			6000	g	0.3 ms half sine pulses. 5 shocks in +/- x,y,z-direction,respectively. (Device unpowered)
Variable Frequency Vibration	f_{VFV}	20		2000	Hz	Tested in +/- x,y,z- direction,50 g peak acceleration.
Package Drop	h_{Drop}			1.2	m	Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.

3.2 Operating Range

Table 3-2 Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	2.1	3.0	3.6	V	
Ambient Temperature	$T_{operating}$	-40		125	°C	Normal operation
	T_{Flash}	-40		125	°C	Flash programming/erasing
	T_{Flash}	-50		150	°C	Without power

3.3 Characteristics

3.3.1 Pressure Sensor

Table 3-3 Pressure Sensor 900kPa Variant

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Pressure Range	$P_{in,H}$	100		900	kPa	
ADC Resolution	$P_{ADC\_res,H}$			1.1	kPa/LSB	
Random Error	$P_{random,H}$	-2.3		2.3	kPa	95% of all measurements
Measurement Error	$P_{Error\ 100\text{-}500,H}$	-5		5	kPa	0°C to +70°C
		-10		10	kPa	-40°C to 0°C,+70°C to +125°C
	$P_{Error\ 500\text{-}900,H}$	-7		7	kPa	0°C to +70°C
		-15		15	kPa	-40°C to 0°C,+70°C to +125°C

3.3.2 Temperature Sensor

Table 3-4 Temperature Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement range	T_{range}	-40		+125	°C	
Measurement error	T_{Error}	-5		+5	°C	-40...-20°C,V_{DD}=2.1…3.6V
		-3		+3	°C	-20...90°C,V_{DD}=2.1…3.6V
		-5		+5	°C	90...+125°C,V_{DD}=2.1…3.6V
Random error	T_{random}	-1		+1	°C	

3.3.3 Battery Sensor

Table 3-5 Battery Sensor

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Measurement range	V_{range}	2.1		3.6	V	
Measurement Error	V_{Error}	-3		+3	%	Percentage of measurement value

3.3.4 Thermal Shutdown

Table 3-6 Thermal Shutdown

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal Shutdown HOT threshold	$T_{HOT,TH}$			125	°C	
Thermal shutdown HOT release	$T_{HOT,RE}$	110			°C	
Hysteresis	T_{HYST}		10		°C	

3.3.5 General Purpose Digital I/O Pins

Table 3-7 Digital I/O Pins - Operating Range

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital Pin Output Current	$I_{in\ DIG}$	-4		4	mA	Pins GPIO0~ GPIO5
Digital Pin Input High Voltage	V_{IH}	$0.8V_{DD}$			V	functional
Digital Pin Input Low Voltage	V_{IL}			$0.2V_{DD}$	V	functional

Table 3-8 Digital I/O Pins - Electrical Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital Pin-Output High Voltage	V_{OH}	$0.8V_{DD}$			V	at 4 mA load current
Digital Pin-Output Low Voltage	V_{OL}			$0.2V_{DD}$	V	
Digital Pin Input Capacitance	C_{in}			10	pF	

3.3.6 Power On Reset and Battery Monitoring

Table 3-9 Power On Reset and Battery Monitoring

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power on Reset level	V_{POR}	1.0		1.6	V	
Power On Reset Release Level	V_{THR}	1.1		1.7	V	
Low Battery Threshold Warning Level	V_{LBAT}	2.2	2.3	2.4	V	

3.3.7 FLASH Memory

Table 3-10 FLASH Memory

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Flash memory data retention time	$t_{Ret\ Flash}$	10			y	Defect rate < 1ppm over lifetime for typical mission temperature profile
Flash write cycles	N_{write}	1000				
Flash page write time	t_{write_line}			7.6	ms	Including time for verification. I2C Baud rate = 400 kbit/s

3.3.8 Supply Currents

Table 3-11 Supply Currents at 3.0V Supply Voltage

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply current in Powerdown state	I_{PWD_3V}		0.2	0.3	μA	+25°C
			2.6	4.5	μA	+125°C
				0.5	μA	-40°C
Supply current in CPU idle state	I_{IDLE_3V}			20	μA	+25°C
			88	152	μA	+125°C
				64	μA	-40°C

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Supply current in Run state	I_{RUN_3V}			0.618	mA	+25°C
				0.576	mA	+125°C
				0.695	mA	-40°C
Supply current in Thermal shutdown state	I_{TSHD_3V}		2.8	4.6	μA	+125°C
Supply current in LF carrier detection mode (digital filter off)	I_{LFCD_3V}			9	μA	+25°C
				12	μA	+125°C
				8	μA	-40°C
Supply current in LF carrier detection mode	$I_{LFCDFilter\_3V}$			9	μA	+25°C
				12	μA	+125°C
				8	μA	-40°C
Supply current in LF data reception mode	I_{LF_3V}			9	μA	+25°C
				12	μA	+125°C
				8	μA	-40°C
Supply current at RF@433MHz - transmission(CW or FSK;CPU off)	I_{RFTX_3V}		5.5		mA	+25°C @5dBm
			8.0		mA	+25°C @8dBm
			11.0		mA	+25°C @10dBm
			5.2		mA	+125°C@5dBm
			7.6		mA	+125°C@8dBm
			10.5		mA	+125°C@10dBm
			5.8		μA	-40°C@5dBm
			8.4		mA	-40°C@8dBm
			11.7		mA	-40°C@10dBm

3.3.9 LF Receiver

Table 3-12 LF Receiver Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
LF Carrier Frequency[1]	f_{LF}	118	125	131	kHz	
LF Data Rate	DR_{LF}	3.8	3.9	4.1	kbit/s	
		6.2	6.5	6.8	kbit/s	
Input differential capacitance	$C_{LF\ diff}$	2.6	4	9	pF	at 125kHz
Input differential resistance	$R_{LF\ diff}$	1			MOhm	
LF Receiver settling time after power on	$t_{ON\_Set.}$			5	ms	After receiver power-on
LF Detection Sensitivity	$S_{nodet.}$	0.1			mVpp	
	$S_{det.}$			2	mVpp	

Note: [1] LF sensitivity levels are only valid for the specified carrier frequency range.

3.3.10 RF Transmitter

Table 3-13 RF1 Transmitter Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Transmit Frequency	$f_{TX,433M,XTAL24M}$	432		444	MHz	XTAL 24MHz
	$f_{TX,433M,XTAL26M}$	433.3		442	MHz	XTAL 26MHz
	$f_{TX,433M,XTAL16M}$	432		448	MHz	XTAL 16MHz
	$f_{TX,315M,XTAL24M}$	312		324	MHz	XTAL 24MHz
	$f_{TX,315M,XTAL26M}$	312		325	MHz	XTAL 26MHz
	$f_{TX,315M,XTAL16M}$	312		320	MHz	XTAL 16MHz
Output Power transformed into 50 ohm	$P_{O,L1,433.92MHz}$		5.6		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=1
	$P_{O,L2,433.92MHz}$		7.7		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=2
	$P_{O,L3,433.92MHz}$		9.8		dBm	V_{bat}=3.0V, T=25°C,Z_{load}=50 ohm RF matched Power Level=3
Output Power change over temp	$dP_{-40℃}$		0.6		dB	V_{bat}=3.0V, T=-40°C
	$dP_{125℃}$		-1.1		dB	V_{bat}=3.0V, T=125°C
Output Power change over supply	$dP_{1.9V}$	-10.1	-7.1		dB	V_{bat}=1.9V, T=25°C
	$dP_{2.1V}$	-5.5	-4.8		dB	V_{bat}=2.1V, T=25°C
	$dP_{3.6V}$	1.6	1.9		dB	V_{bat}=3.6V, T=25°C
RF Datarate	DR_{RF}			19.6	Kbit/s	Manchester coded
RF Data Rate tolerance	dDR_{RF}	-1		+1	%	
FSK frequency shift			+/-45	±70	KHz	Programmable
RF Data Duty Cycle	$DC_{RF,ASK}$	45	50	55	%	Valid only for ASK or FSK
ASK Mod depth	$MD_{RF,ASK}$	90			%	

Table 3-14 RF1 Crystal Oscillator

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Crystal Frequency	f_{XTAL}		16/24/26		MHz	
Crystal Oscillator startup peak current	$I_{Xtal\_start\_peak}$	0.5			mA	
Crystal Oscillator startup time	t_{Xtal_start}			2	ms	

3.3.11 Wake-up and power-on timing

Table 3-15 Wake-up and power-on timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power on time	t_{ini}			15	ms	From the power on to the user program began to run
Resume from System idle time	t_{resume}			100	μs	Time from resume event during system-idle to application code execution start.
LF Wake-up time	$t_{LF\ wake\text{-}up}$			5	ms	Time from LF wake-up event during power-down to application code execution start.
Watchdog Wake-up time	$t_{wd\ wake\text{-}up}$			5	ms	Time from watchdog timer elapsed during power-down to application code execution start.

4 Operating Modes and States

4.1 Operating Modes

The SNP739D provides three operating modes: normal mode, debug mode, programming mode/download mode. The operating mode is decided by GPIO0, GPIO1 power strapping. Operating mode will be latched at positive edge of power on reset (POR). And GPIO1, GPIO0 should be held at least 256ms for stable operating mode generation.

Table 4-1 Operating Modes Overview

GPIO1	GPIO0	Short Description
0	1	Debug mode[1]
1	0	Programming mode/Download mode[2]
1	1	Normal mode[3]
0	0	Reserved

Note:
[1] Debug mode: used for chip debugging.
[2] Programming /Download mode: Used for firmware download.
[3] Working status in Normal mode: 1.Init. 2.Run. 3.CPU idle. 4.Powerdown. 5.Thermal shutdown.

4.2 Device states

In normal operation mode the SNP739D can be switched into several device states which differ in the number of enabled circuit blocks. For lowest power consumption unused blocks are disconnected from power supply, hence not even idle currents remain.

Table 4-2 Device states overview

Device state	Short description	Important activated blocks
Init	Enter Init state when system reset is active.	See Table 4-3 Power management
Run	Application code execution.	See Table 4-3 Power management
CPU idle	CPU clock is stopped to reduce the current consumption, any peripheral interrupt, such as Timer1/Timer2/Timer3/Timer8/SPI/ I2C/UART, ADC, RF Transmitter or LF receiver can wakeup CPU to Run state.	See Table 4-3 Power management
Powerdown	No code execution. Device is waiting for a wake-up event. Lowest current consumption.	See Table 4-3 Power management
Thermal shutdown	Once the system enters Shutdown state it would resume running only when the TMAX circuit temperature is below TMAX threshold setting first, then wake-up timer reset is active.	See Table 4-3 Power management

Table 4-3 Power management

Block Name	Run	CPU Idle	Powerdown/Shutdown
POR	Active	Active	Active
Low battery monitor	Active	Active	Inactive
TMAX detector	Inactive/Active (Selectable)	Inactive/Active (Selectable)	Inactive
Voltage regulator	Active	Active	No supply

Block Name	Run	CPU Idle	Powerdown/Shutdown
Power management/wake-up timer	Active	Active	Active
CPU	Active	Inactive	No supply
Peripheral CRC, I2C,SPI, LIN, UART,LF decoder, RF encoder	Active	Active	No supply
Timer 1,2,3,8	Active	Active	No supply
256 Bytes IRAM	Active	Active	No supply
128 Bytes XRAM	Active	Active	Inactive
FLASH	Active	Active	No supply
ROM	Active	Active	No supply
Crystal oscillator (24MHz/16MHz/26MHz)	Active	Active	No supply
1k/39kHz RC oscillator	Active	Active	Active
2MHz RC oscillator	Active	Active	No supply
LF interval timer	Active	Active	Inactive/Active (Selectable)
LF receiver	Active	Active	Inactive/Active (Selectable)
RF transmitter	Active	Active	No supply

Note: **Active**: block is powered, active and keeps its register contents; **Inactive**: block is powered, cannot be used, but keeps it register contents;**No supply**: block is not powered, cannot be used and all register content is lost.

4.3 State Transitions

Figure 4-1 shows the possible state transitions in normal mode. The central device state is Run state because only in Run state the state transitions can be configured. Entering other states from Run state is controlled by application code, either by calling firmware functions or setting control bits. State transitions from other states are controlled by hardware events, e.g. timer events or LF receiver events.

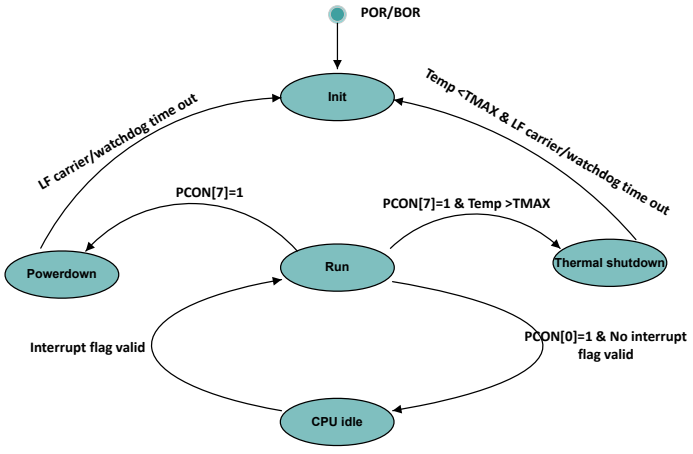


Figure 4-1 State transitions

Note: The system can be wakeup from CPU idle to Run state by any interrupt.

5 Functional Descriptions

5.1 Block Diagram

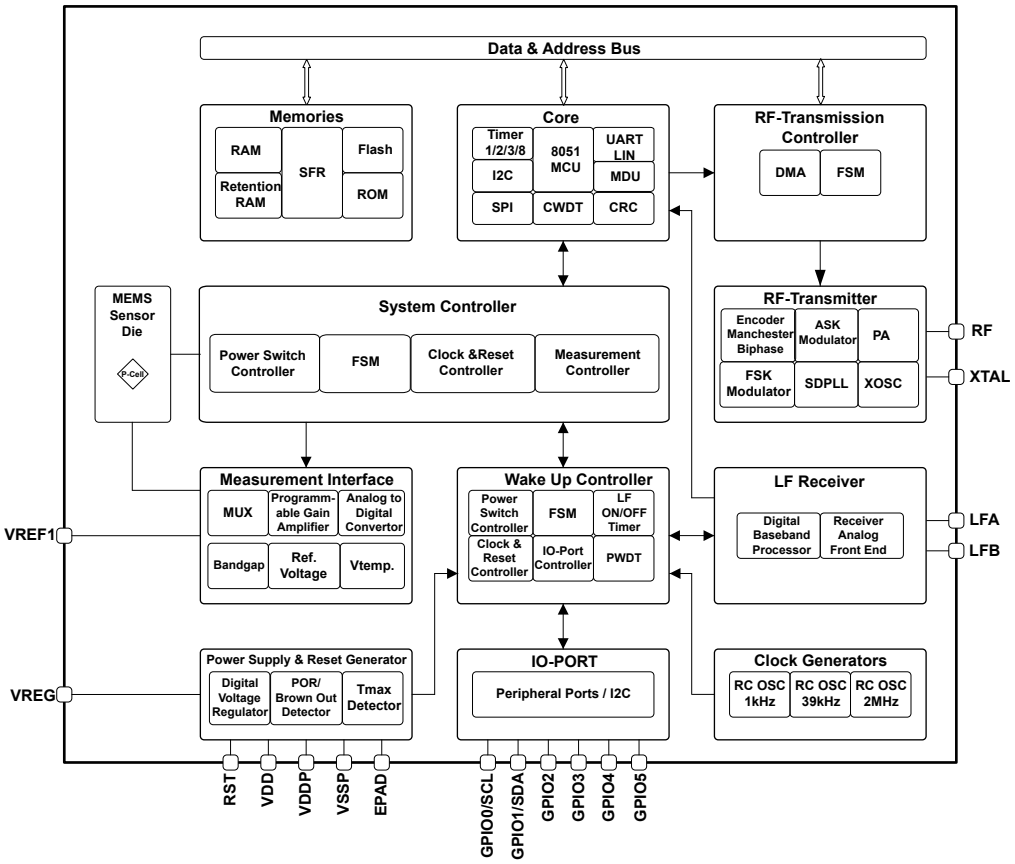


Figure 5-1 Block Diagram

5.2 Wake-up Controller

In a typical TPMS application the SNP73X is in Powerdown state most of its lifetime. In Powerdown state, which is triggered by calling the firmware function LIB_PDWN_MODE(), the device is controlled only by the wake-up controller. The wake-up controller is the block with highest priority in terms of power management. It is always powered and waits for a wake-up event from different sources. For lowest power consumption the wake-up controller is clocked by the 1 kHz oscillator. If a wake-up event happens and the event is not masked then the wake-up controller powers on the system controller which takes over device control. Before code execution starts the CPU runs a firmware boot sequence and all registers are initialized with their wake-up values. In the case of normal mode the time from wake-up event occurrence until start of application code execution is in the range of several milliseconds. The implemented wake-up sources are:

- Period Wakeup timer (PWDT)
- LF-Receiver: carrier detector
- LF-Receiver: wakeup ID matching circuit

- General purpose I/O (GPIO0~ GPIO5 configurable)
- TMAX detector when device is in Thermal shutdown

The second main function of the wake-up controller is reset handling. The reset signals are generated in the block “power supply and reset generator”. A system-reset may be trigged by:

- Brown out (internal regulated voltage drops below a certain threshold)
- Power on
- Software
- Period wakeup timer underflow

When Power on reset or Brown out reset occurs, all logic will be reset. After reset release, the chip work mode will be decided by the value of GPIO0 and GPIO1(see Charpter 4.1). Period wakeup timer reset and software reset will not change chip work mode selection.

Furthermore, the wake-up controller comprises the LF ON-OFF timer that allows operating the LF-receiver with a configurable duty cycle for power saving reasons.

5.2.1 Period wakeup Timer (PWDT)

The PWDT is a 16-bit timer (SFRs PWDTH and PWDTL). The main function is to periodically wake-up the device from power down. The timer is active in any low power state and is clocked by the 4kHz oscillator divided by 8 or 512 (SFR bit PMU_PWDT_SEL). The PWDT is counting down, a wake-up event is triggered upon timer underflow. The PWDT should be properly configured to avoid interrupting the telegram transmission or the data acquisition.

Note that the PWDT is set to 0xFFFF after underflow.

The associated registers are:

- PWDTH, PWDTL: PWDT counter
- TCONL.PMU_PWDT_SEL: Setting this bit selects the PWDT clock division value

5.2.2 LF ON-OFF Timer

The ON-OFF timer is used for switching the LF receiver on and off with a low duty cycle in order to save energy. The ON-timer is an 8-bit timer, and the OFF-timer is a 12-bit timer. Both the ON-timer and OFF-timer are clocked by 1kHz oscillator. Consequently, the timer supports long OFF-times of up to 4 seconds and shorter ON-times of maximal 0.256 second.

The user does not need to directly access the ON-OFF timer registers since the firmware function LIB_LFLP_ONOFF_CFG() can be used for configuration. Setting bits LF_LP_MODE and LF_WAKE_EN activates the ON-OFF timer. The current count value of the ON-OFF timer cannot be read by software.

Associated registers:

- PCON, bits LF_WAKE_EN
- LF_LP_CFG0, bits LF_LP_MODE

5.2.3 LF Receiver Wake-up/Resume Events

The LF receiver wake-up events are:

- Carrier detected
- Wake-up pattern match

5.2.4 General Purpose I/O Wake-up/Resume Event

All I/O Ports (GPIO0~GPIO5) can be configured as an external wake-up source. In order to use this wake-up source, the corresponding GPIO needs to be configured as input (SFR bits GPIO0DIR~GPIO5DIR=1), the corresponding pull resistor must be enabled (SFR bits GPIO0_PUPD~GPIO5_PUPD=0) and the corresponding wake-up must be enabled (SFR bits IO0_WAKE_FLAG_EN=1 and IO1_WAKE_FLAG_EN=1) and the corresponding wake-up I/O must be selected(WAKE_IO_SEL[1:0]).

Note: Note that the General purpose I/O wake-up is triggered on low level only.

Table 5-1 Truth Table of Wake-Up I/O Selection

GPIOnDIR	GPIOn_PUPD	GPIOnOUT	IO0_WAKE_FLAG_EN (GPIODIR[7])	IO1_WAKE_FLAG_EN (GPIODIR[6])	WAKE_IO_SEL[1:0] (GPIODATN[7:6])	Selected wake-up I/O
1	0	1	0	0	Ignore	Disable
1	0	1	0	1	00	GPIO2
1	0	1	0	1	01	GPIO3
1	0	1	0	1	10	GPIO5
1	0	1	0	1	11	GPIO2 GPIO3 GPIO5
1	0	1	1	0	00	GPIO0
1	0	1	1	0	01	GPIO1
1	0	1	1	0	10	GPIO4
1	0	1	1	0	11	GPIO0 GPIO1 GPIO5
1	0	1	1	1	00	GPIO0 GPIO2
1	0	1	1	1	01	GPIO1 GPIO3
1	0	1	1	1	10	GPIO4 GPIO5
1	0	1	1	1	11	GPIO0~ GPIO5

Associated registers:

- GPIODIR, GPIO input or output selection
- GPIOPUPD, GPIO wake-up enable and pullup/pulldown selection
- GPIODATN, bits WAKE_IO_SEL[1:0], Wake-up I/O selection

5.2.5 Power-On and Under-Voltage Reset

Figure 5-2 shows the device behavior depending on voltage at VDD pin. If the voltage falls below a certain threshold V_{POR} a system-reset is triggered. The device stays in reset until the voltage at VDD pin exceeds the reset release threshold V_{THR}. After reset release the device initialization is started which takes a certain time, t_{ini}. After the initialization phase the operation mode of the device can be selected by strapping the GPIO0 and GPIO1.

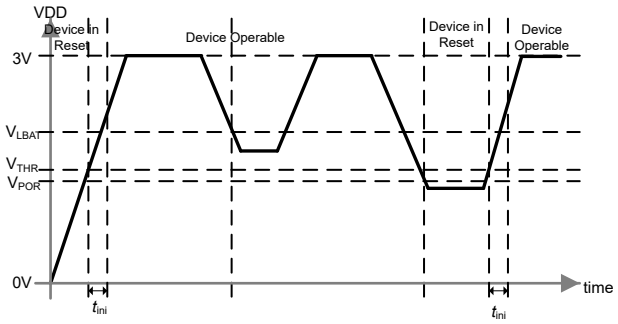


Figure 5-2 Power-On and Under-Voltage Reset Behavior

5.2.6 Software Reset

After a reset triggered by software the device runs through the reset boot sequence. The software reset can be triggered by setting the bit RESET (located in register EPCON) in application code. Software reset mainly focus on reset in Normal mode or Debug mode, and it will reset Core and System Controller block, and the chip mode selection is not affected.

Associated registers:

- EPCON(bit RESET for triggering software reset)

5.2.7 Thermal Shutdown

Thermal shutdown function is enabled by setting the bit TSHDWN_EN (located in register PCON) in application code, and the TMAX detector is active when TSHDWN_EN=1. A flag TGOOD (location in register EPCON) is keep high level if the temperature is below the hot temperature threshold Thot_th. If the temperature is above hot temperature threshold Thot_th, the flag TGOOD is pulled down by TMAX detector, so the application code can polling the flag TGOOD, then enter Thermal shutdown by setting the bit PDWN(location in register PCON). Once in Thermal shutdown the device is only release if the on-chip TMAX detector indicates a temperature below the hot release temperature Thot_re. After release from Thermal shutdown a wake-up is performed.

Associated registers:

- EPCON (bit TGOOD for indicating TMAX detector)
- PCON (bit TSHDWN_EN for enable TMAX detector, bit PDWN for enter Thermal shutdown)

5.3 System Controller

Main function of the system controller is power management after device wake-up from power-down or device resume from CPU idle. Unlike the wake-up controller most other circuits can be disconnected from power individually. Depending on the device state the system controller connects the required blocks to the power domain. Here the device states are listed, ordered by current consumption, starting with the state with highest current consumption:

- Run state
- CPU idle state (Run state with CPU disconnected from system clock)
- Powerdown state (optional with LF receiver enabled)

5.3.1 Measurement Controller

Refer to the associated firmware function:

- LIB_MEAS_PRESSURE()
- LIB_MEAS_TEMPERATURE()
- LIB_MEAS_VOLTAGE()

5.4 Clock Generators

The SNP73X comprises three on-chip RC oscillators in order to fulfill the extremely different requirements in terms of power consumption and cycle time for different operating states. A 1kHz oscillator is operated in power-down for lowest power consumption. A 39kHz oscillator is implemented for clocking the system controller and the digital part of the LF receiver. Finally, a 2MHz oscillator is mainly used for the ADC. The 2MHz clock may be divided (controlled by bit field SYSCLKDIV). The 39kHz oscillator is trimmed in production. However, the user can use the associated firmware function to calibration all the three on-chip RC oscillators if needed.

All the three on-chip RC oscillators can be configured as system clock for CPU (controlled by bit field SYSCLKSEL).

Attention: Note that the 1kHz and 39kHz oscillator cannot be enabled simultaneously.

For RF transmission and calibration purposes a crystal oscillator (XTAL) is implemented as well. The XTAL can also used as system clock by configuring the SFR bits SYSCLKSEL and can be divided by configuring the SFR bits SYSCLKDIV.

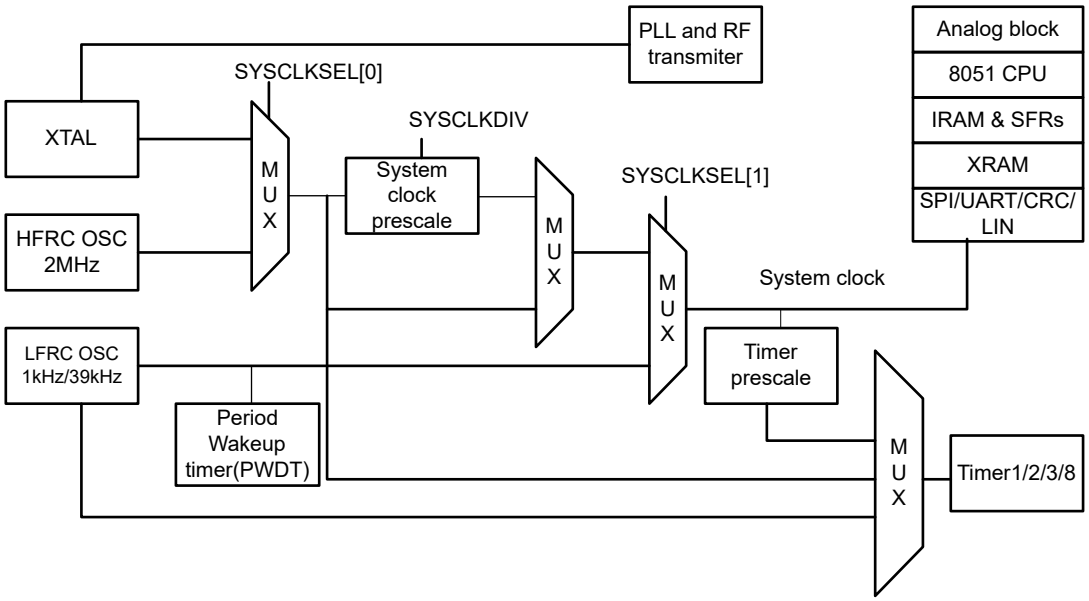


Figure 5-3 Clock distribution diagram.

Associated registers:

- SYSCLKSEL (system clock selection)
- SYSCLKDIV (XTAL or RC OSC 2MHz clock division)

Associated registers:

- LIB_HF_CLK_CAL()
- LIB_PD_CLK_CAL()
- LIB_LF_CLK_CAL()
- LIB_SYSCLK_SEL()
- LIB_HFOSC_START()
- LIB_HFOSC_STOP()
- LIB_XTAL_OSC_START()
- LIB_XTAL_OSC_STOP()

5.5 Core

The Core comprises an 1T cycle 8051 based MCU and the following peripherals:

- Timer Module
- Hardware CRC
- Core watchdog timer (CWDT)
- Multiplication-Division Unit (MDU)
- UART/LIN interface
- SPI interface

5.5.1 Timer Module

There are 4 general purpose counters with 16 bits, Timer1/Timer2/Timer3/Timer8.

- **Timer1**

  This timer is a 16 bits counter. It counts down from the value previously loaded into the counter and stops when it reaches zero. The counter will not wrap around, so a new value must be written into T1L and T1H to start a new period count, and these values will be loaded on timer1 enable.

- **Timer2**

  This timer is a 16 bits counter which can count-down or count-up. The following list is its work mode:

  1. **mode 0**: 16 bits decrease counter. In this mode, source clock is decided by SFR TCONL configure (system clock divided by 16 or 128). If the counter reaches zero, an all-zero detect will trigger on the next falling edge of the clock (which will stop the clock in the clock block).
  2. **mode 1:** used as ADC data accumulator. During ADC working on, please not take timer2 as other normal usage.
  3. **mode 2:** used as pseudo-random generator.
  4. **mode 3:** 16 bits increment counter. In this mode source clock is decided by SFR TCONL configure. When RC OSC 1kHz/39kHz calibration bit (TCONL[4]) or RC OSC 2MHz calibration bit is set (TCONL[3]) is set then the source clock will switch to XTAL by hardware automatically. All-zero detect is disabled in this mode but the counter will stop when Timer1 reaches zero (this operation is crucial for the correct calibration of the 1kHz/39kHz and 2MHz clock). In certain situations, the interrupt from Timer1 should also stop the clock of Timer2.

- **Timer3**

  This is a 16 bits counter that can be used as a down counter.

  When Timer3 is used as 16-bit down counter, the source clock is decided by SFR bit FAST_T3, and if the counter reaches zero, SFR bit T3_FULL will be set by hardware. In order to clear this interrupt, T3_ON should be off.

  > **Note:** Note that the timer3 is used as baud-rate generator for UART transmission when UART is enabled.

- **Timer8**

  This timer is a 16 bits counter which supports input capture, output compare and the generation of PWM. The main function of timer8 is as follows:

  - Configurable up or up-down counter with initial and final value.
  - Configurable input capture on rising edges, falling edges or both edges.
  - Configurable output compare mode the output signal be set, cleared or toggled on match.
  - Configurable PWM for center-aligned PWM or edge-aligned PWM with deadtime insertion.

Associated registers for timer1/2/3:

- TCONH, TCONL
- TH1, TL1

- TH2, TL2
- TH3, TL3
- INTL (timer1/2/3 interrupt flag)

5.5.2 Hardware CRC

This module is a generic re-configurable CRC calculator for calculating the CRC of a variable length data sequence. The CRC order (up to 16), polynomial and initial value can be configured by the application.

The CRC is calculated on 8/16 bits basis, therefore the application must break up a long message into individual words and feed these to the calculator sequentially. The intermediate CRC value can be read from SFR CRCH/CRCL after each data input done.

- **CRC function:**
  - **STEP1:** initial CRC setting.

    Write 0x0000 to the CRC Generator Polynomial register (CRCPOLYH, CRCPOLYL)

    Write 0x000F to the CRC Configuration register (CRCCON)

    Write the initial CRC value to the CRC register (CRCH, CRCL)

    Write polynomial to SFR CRCPOLYH, CRCPOLYL.

  - **STEP2:**

    Configure the module by writing the CRC order (eg. CRC16) and the message remainder fields of the CRC configuration register (CRCCON).

  - **STEP3:**

    Write the message to SFR CRCH/CRCL in sequence (MSB first).

    Must send CRCH then CRCL.

  - **STEP4:**

    Update the CRC message remainder field of the SFR CRCCON with the remaining number of bits to process. Write the last message word to the CRC register.

  - **STEP5:**

    Read the final computed CRC value from the CRC register (CRCH, CRCL).

With hardware CRC associated registers:

- CRCPOLYL
- CRCPOLYH
- CRCCON
- CRCL

- CRCH

5.5.3 Core watchdog timer (CWDT)

A count down core watchdog timer (CWDT) using the free running clock offers configurable and robust protection against application lock-up.

The CWDT will generate a system reset when the firmware runs in abnormal loops, the Program Counter will be reset to 0x0000. In order to prevent the reset from CWDT, the firmware should reset the CWDT timer periodically.

Table 5-2 CWDT period config

CWDT_CLK_SEL	CWDT_OV_SLE[2:0]			Clock source	Overflow time
0	0	0	0	LFRC	2^5*T(1kHz)
0	0	0	1	LFRC	2^6 *T(1kHz)
0	0	1	0	LFRC	2^7 *T(1khz)
0	0	1	1	LFRC	2^8 *T(1kHz)
0	1	0	0	LFRC	2^9 *T(1kHz)
0	1	0	1	LFRC	2^10*T(1kHz)
0	1	1	0	LFRC	2^11*T(1kHz)
0	1	1	1	LFRC	2^12*T(1kHz)
1	0	0	0	System clock	2^13 * T(sysclk)
1	0	0	1	System clock	2^14 * T(sysclk)
1	0	1	0	System clock	2^15 * T(sysclk)
1	0	1	1	System clock	2^16 * T(sysclk)
1	1	0	0	System clock	2^17 * T(sysclk)
1	1	0	1	System clock	2^18 * T(sysclk)
1	1	1	0	System clock	2^19 * T(sysclk)
1	1	1	1	System clock	2^20 * T(sysclk)

Associated registers:

- TCONH (bits CWDT_EN, CWDT_CLK_SEL, CWDT_OV_SEL)
- EPCON (bit CWDT_RST)

5.5.4 Multiplication-Division Unit (MDU)

The MDU provides 32-bit division, 16-bit multiplication, shift and normalize operations. All operations are unsigned integer operations.

Refer to “SNP739D_Reference_Manual” for MDU details usage.

5.5.5 I2C Controller

The SNP739D features a slave hardware I2C interface with the fixed device address 0x6C. When the I2C is activated, pin GPIO0 is configured as input and serves as clock line (SCL). Pin GPIO1 is initialized as input, too, and serves as data line (SDA). Both lines need a pull-up resistor, either an external resistor or by activating the internal pullup resistors. The active device transmits data by pulling the data line low.

In program-mode and debug-mode the I2C interface is managed by an I2C firmware . Only certain I2C commands are available in these modes, no application code can be executed. The internal pull-up resistors are enabled by the I2C handler.

In normal mode the I2C (if needed) must be managed by application code. For activating the I2C interface the bit I2CEN must be set. The internal pull-up resistors are automatically set for GPIO0 and GPIO1. The port direction register is managed automatically by the I2C interface.

Receiving data from master in normal mode

Once activated, the I2C register waits for a start condition. The following 8 bits are interpreted as device address and compared to 0x6C. If the received address matches, acknowledge (ACK) is generated, i.e. the data line is pulled down on the 9th clock pulse. The next 8 bits are interpreted as data bits and are also acknowledged by pulling the data line low. The complete reception of a data byte is indicated by the flag RXRDY. The application code needs to poll this flag and fetch the data from the register I2CD. RXRDY must be cleared by firmware write 0 to it. This procedure is repeated for incoming data bytes until a stop condition is received. If the I2C event interrupt is enabled, the receiver raises an interrupt on every received byte from the I2C bus.

Transmitting data from SNP739D to master in normal mode

The LSB of the device address serves as a read-write indicator. Thus, in order to put the SNP739D in data transmission mode, the master must send the device address 0x6D.

A transmit data buffer is used for I2C transmitting data, and it only supports the transmission of two bytes messages from the chip. The TXRESET status bit must be cleared for the transmit data buffer and the two bytes data that make up the message should then be written into the buffer by the firmware. When a two-byte data has been transmitted, the TXDONE bit is set. If the I2C event interrupt is enabled, the TXDONE interrupt will only be raised for a two (or more) bytes read and once raised will not occur again until the status bit TXRESET has been cleared by the firmware.

Note: Note that the system clock should be at least 2 times faster than I2C master clock.

Associated registers:

- I2CS
- I2CD
- I2CEN

5.5.6 UART/LIN Interface

The SNP739D has a hardware UART/LIN interface. If enabled, pin GPIO3 serves as UART-TX and GPIO4 as UART-RX. The device embeds two universal synchronous/asynchronous receivers /transmitters which communicate at speeds of up to 2 Mbit/s.

Table 5-3 UART mode selection

MSEL0	MSEL1	Mode	Description	Baud rate
0	0	Mode 0	Shift register	SYSCLK/12
0	1	Mode 1	8-bit UART	Variable
1	0	Mode 2	9-bit UART	Variable

MSEL0	MSEL1	Mode	Description	Baud rate
1	1	Mode 3	9-bit UART	Same as Mode2

$$BaudRate = \frac{f_{SYS\_clk}}{T3L+1}$$

In mode 0 the Serial Port 0 operates as synchronous transmitter/receiver.8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the main clock frequency. Transmission is started by writing data to UARTBUF register.

In mode 1 the UART operates as asynchronous transmitter/receiver with 8 data bits and programmable baud rate.

Timer 3 T3L used to generate baud rate. Transmission is started by writing to the UARTBUF register. The first bit transmitted is a start bit (always 0), then 8 bits of data proceed, after which a stop bit (always 1) is transmitted.

In mode 2 or mode 3 the Serial Port 0 operates as asynchronous transmitter/receiver with 9 data bits and programmable baud rate. Additionally, the baud rate can be doubled with the use of the SMOD bit of the SYSCON3[3] register. Transmission is started by writing to the UARTBUF register.

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0 can be used for multiprocessor communication.

LIN mode is active when LIN_EN=1(SFR bit UARTCON1[0]), the mode selection bits MSEL0/MSEL1 should be set to ‘01’ (mode1).

The LIN transmission is firstly started with a break character which sending 13-bit ‘0’ and 1-bit ‘1’ by set LBRK_SEND_EN=1, and LBRK_SEND_EN will be reset to ‘0’ after the break character transmit finished. Following the break character, a new byte data will be transmitted by writing the UARTBUF register which is the same as UART mode1 transmission.

The LIN receive is enabled by set REN=1. A break character flag (LBRK_FLAG) is raised by hardware when a continuous 10-bit or 11-bit ‘0’ is detected. After detection of LIN break character, the firmware can continue to receive the coming data bytes which is the same as UART mode1 receive.

Associated registers:

- UARTCON0
- UARTCON1
- UARTBUF
- SYSCON0(bit UART_EN)

5.5.7 SPI Interface

The SPI may be programmed to work as master or as slave device.

- Full duplex mode
- Master or Slave mode
- Four SPI Master baud rates

- Slave Clock rate up to Fclkper/4
- Serial clock with programmable polarity and phase
- Master Mode fault error flag with interrupt capability
- Write collision flag protection
- Programmable 8-bit data transmitted Most Significant Bit (MSB) first or Least Significant Bit(LSB) first
- DMA mode up to 64-byte data transmitted and slave select (ssn) output
- Bi-directional mode

In master mode the SPI waits on write operation to “SPIDAT” register. If write operation to “SPIDAT” register is done, transmission is started. Data shifts out on “mosio” pin at the “scko” serial clock transition (“send_edge”). Simultaneously, another data byte shifts in from the slave on master's “misoi” pin (“capture_edge”).

In slave mode the SPI waits on low level on “ssn” input. The “ssn” input must remain low until the transmission is completed. The beginning of transmission depends on the state of the “SPI_CPHA” bit of SPCON1 register. When “SPI_CPHA” is cleared, then the slave must begin driving its data before the first “scki” edge, and a falling edge on the “ssn” input is used to start the transmission. When the “SPI_CHPA” bit is set, then the slave uses the first edge of “scki” input as a transmission start signal.

The SPI interrupt request can be caused by the “spif” flag and “modf” flag. When the transmission ends the “spif” flag is set automatically by hardware. The “modf” flag is set automatically by hardware when level on the “ssn” input is inconsistent with respect to the selected operation mode (the SPI is configured in master mode and there is low level detected at “ssn” input) and the “ssdis” flag is cleared. The interrupt request is disabled when both flags “spif” and “modf” are cleared.

The DMA mode is enabled when “SPI_DMA_EN=1”, and the SPI uses RAM address from 0x80 to 0xBF as transmit buffer and uses RAM address from 0xC0 to 0xFF as receive buffer. The number of data transmitted can be configured by setting “SPIDAT[7:2]” and the interval of two bytes data transmitted can be configured by setting “SPIDAT[1:0]”. The “spif” is set by hardware When transmit finished. In Master mode, “ssn” is output to Slave device when “ssndis=1” during DMA mode transmitting.

The Bi-directional mode is enabled when “BIDIR_MODE=1”. In this mode, the SPI uses only one serial data pin for the interface with external device. In the master mode, the GPIO3 becomes the serial data I/O, and the direction of GPIO3 is controlled by GPIO3DIR (GPIODIR[3]); In the slave mode, the GPIO4 becomes the serial data I/O, and the direction of GPIO4 is controlled by GPIO4DIR (GPIODIR[4]).In the bi-directional mode, the GPIO4 in master mode and the GPIO3 in slave mode are not occupied by the SPI, and can be used for other purpose in this case.

Associated registers:

- SPICON0
- SPICON1
- SPIDAT
- SYSCON0(bit SPI_EN)

5.6 Memories

The 8051 based microcontroller core is able to address a 64KB wide range of code memory. In the SNP739D this address range is used for the following types of memory:

- 640 Bytes Flash memory for factory configuration1 data
- 512 Bytes Flash memory for factory configuration2 data
- 512 Bytes Flash memory for user configuration data (user configuration sector)
- 16 KB Flash memory for Application code (user code sector)
- 32 KB ROM memory for Rom-Library code
- 128 Bytes Retention RAM (XRAM)
- 256 Bytes Data RAM (IRAM)

The content of factory configuration1 and factory configuration2 sector cannot be changed. The factory configuration1 sectors is protected against reading by lockbyte1, and the factory configuration2 sectors is protected against reading by lockbyte4, both lockbyte1 and lockbyte4 are factory set.

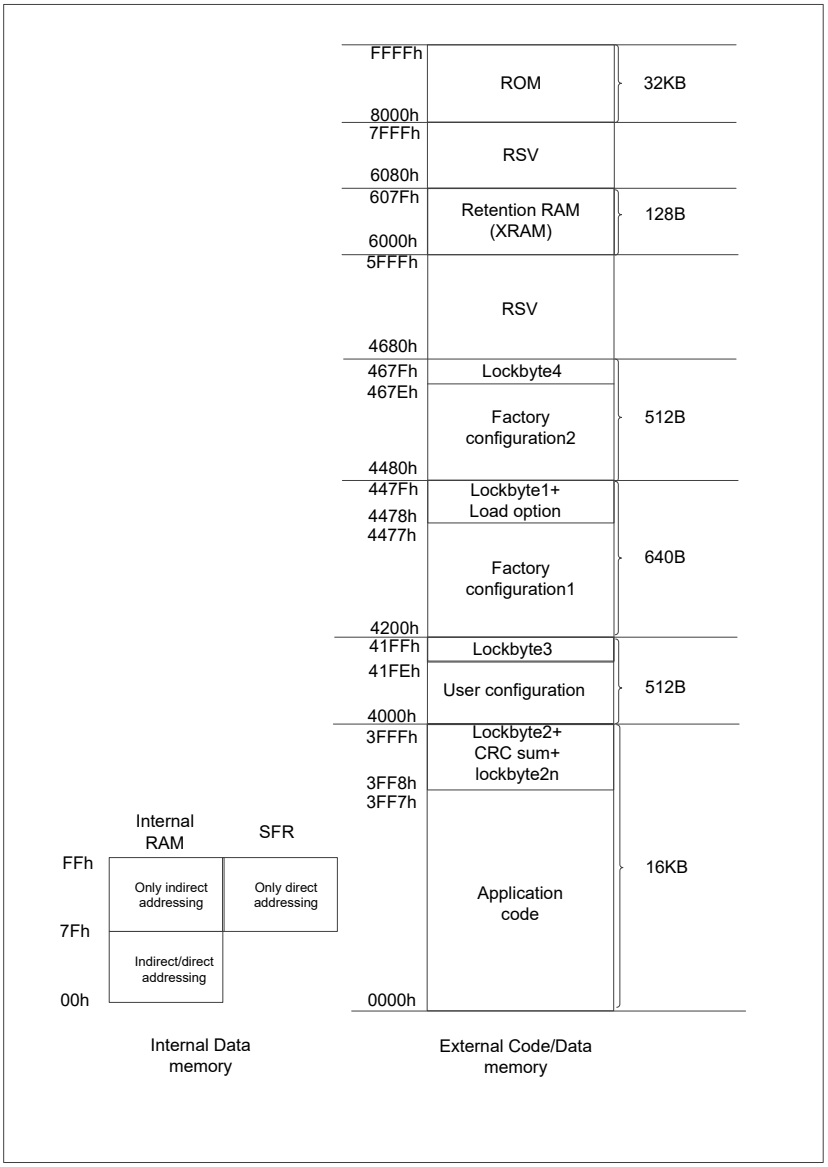


Figure 5-4 Memory map

5.6.1 Lock-byte

At the end of each flash sector there is a lock-byte, which may be enabled by the user in order to protect the sector against overwriting and reading.

Setting the lock-byte to 0xFF will result in an unlocked FLASH area, any other value must not be written to these locations. After programming a valid lock byte value, the new lock byte takes effect after the next system reset occurs.

Lockbyte1(LB1):

This lock byte protects the FLASH sectors factory configure against overwriting and erasing.

Lockbyte2(LB2) and lockbyte2n(LB2n):

These two lock-bytes protect the FLASH main code against overwriting, erasing (except limited internal production test mode) and read-out to prevent reverse engineering of the application code.

These two lock-bytes must be set at the end of the programming sequence of the code sector via the I2C interface. Once set, the available operating modes are limited.

The FLASH main area is organized into 32 pages (page0~page31) of 512-bytes each. The lockbyte2 protects the FLASH main range from lower pages to upper pages, but the lockbyte2n protects the FLASH main range from upper pages to lower pages. Once lockbyte2 or lockbyte2n is not 0xff, the last page (page31) is always locked. Table 5-4 shows the lockbyte2 for lock range of FLASH main, and Table 5-5 shows the lockbyte2n for lock range of FLASH main.

Table 5-4 Lockbyte2 for lock range of FLASH main

Lockbyte2 value	Locked range of FLASH main	Locked address of FLASH main
0xff	unlocked	none
0xfe	Page0 and page31	0x0000~0x01ff and 0x3e00~0x3fff
0xfd	Page0~page1 and page31	0x0000~0x03ff and 0x3e00~0x3fff
0xfc	Page0~page2 and page31	0x0000~0x05ff and 0x3e00~0x3fff
…	Page0~pageN and page31	0x0000~[0x0200 * hex(N)+0x01ff] and 0x3e00~0x3fff
0x80	Page0~page31	0x0000~0x3fff
0x00~0x7f	Not used, DON'T set	Not used, DON'T set

Table 5-5 Lockbyte2n for lock range of FLASH main

Lockbyte2n value	Locked range of FLASH main	Locked address of FLASH main
0xff	unlocked	none
0xfe	Page31	0x3c00~0x3fff
0xfd	Page30~page31	0x3a00~0x3fff
0xfc	Page29~page31	0x3800~0x3fff
…	PageN~page31	[0x0200 * hex(N)] ~0x3fff
0x80	Page0~page31	0x0000~0x3fff
0x00~0x7f	Not used, DON'T set	Not used, DON'T set

Note: Where N is given from 0 to 31, and hex(N) denotes the hexadecimal value of N.

Lockbyte3(LB3):

This lock byte protects the FLASH sector (user configuration sector) against overwriting and erasing (except limited internal production test mode).

This lock byte can be set either via I2C in PROGRAMMING mode in same programming sequence as lockbyte2 is set, or by using a dedicated library function in NORMAL mode by the software.

Table 5-6 shows the possible lock-byte settings and their effect on the flash sectors for program mode and normal mode.

Table 5-6 Protected Flash

Protected Flash sectors	lockbyte2 and lockbyte2n	lockbyte3	Values		Unit	
			user code	user config	user code	user config
none	0xFF	0xFF	R: yes W: yes SE: yes CE: no	R: yes W: yes SE: yes	R: yes W: yes SE: yes CE: yes	R: yes W: yes SE: yes
user code	not 0xFF	0xFF	R: yes W: no SE: no CE: no	R: yes W: yes SE: yes	R: no W: no SE: no CE: yes	R: yes W: yes SE: yes
user config	0xFF	0x00	R: yes W: yes SE: yes CE: no	R: yes W: no SE: no	R: yes W: yes SE: yes CE: yes	R: yes W: no SE: no
user code/user config	not 0xFF	0x00	R: yes W: no SE: no CE: no	R: yes W: no SE: no	R: no W: no SE: no CE: yes	R: yes W: no SE: no

Note: [1] **R:** Read; [2] **W:** Write; [3] **SE:** Sector Erase; [4] **CE:** Chip Erase.

5.6.2 Flash Programming

For programming the user code sector or the user configuration sector in program mode there are two I2C commands available. The command Erase-Sectors for deleting the sectors as a whole and the command Flash-Write-Line for programming a 64-byte long flash line. For enabling the lock-bytes LB3 the value of the lock-byte location must be defined as 0x00 when writing to the corresponding line with the Flash-Write-Line command. The lock-byte LB2 and LB2n must be proper defined depend on the corresponding sector that need to be locked. If a lock-byte shall remain disabled, its value must be defined as 0xFF.

For programming the user configuration sector in normal mode, i.e. during runtime, the firmware functions LIB_FLASH_WRITE() are available.

Attention: Note that the system clock must be switched to 2MHz before calling this firmware function.

5.6.3 ROM

The ROM has 32K bytes totally, it is used as store the firmware library.

5.6.4 Retention RAM(XRAM)

In order to save information when the device is in a low power state or in Thermal shutdown there are 128 Bytes of retention RAM available. The retention RAM is mapped to the external RAM address space of the 8051 CPU. Hence, in a C environment, the directive XDATA must be used to define a variable located in retention RAM area.

The retention RAM has random values after power-on, i.e. Enabled retention RAM will keep its values in all device states as long as the device is connected to the battery.

5.6.5 Data RAM(IRAM) and SFRs

The microcontroller core has a 256 Byte address space for data RAM that can be used in application code. The address space 0x80 to 0xFF of the upper 128 Bytes of data RAM is shared with the Special Function Register (SFR) bank. The two register banks are selected via addressing method. If direct addressing is used a SFR is selected, if indirect addressing is used data RAM is selected. The RAM in the lower addressing range can be accessed either by direct or indirect addressing. This is illustrated in Figure 5-5.

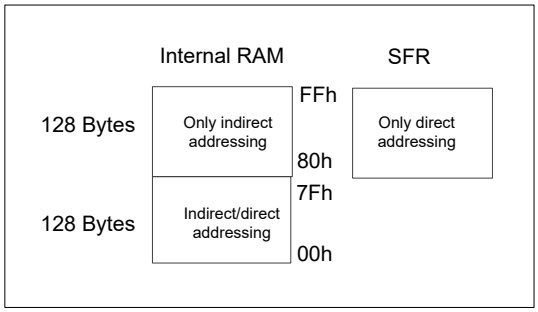


Figure 5-5 RAM/SFR map

5.7 Power Supply and Reset Generator

The Power Supply and Reset Generator provides the power for different voltage domains:

- Analog domain
- Digital domain
- Retention RAM

Furthermore, this functional block provides a reset signal on power-on and under-voltage for the wake-up controller (see Chapter 5.2.5).

Note: A external capacitor must be connected to VDDREG-pin in order to stabilize the internal voltage. This pin must not be used as voltage supply for external devices.

5.8 Measurement Interface

The measurement interface block is the interface between the analog sensor signals and the digital signal conditioning domain. A multiplexer selects one of the following input signals for the 12-bit analog to digital converter:

- Pressure Sensor (located on separate MEMS chip)
- Temperature Sensor
- Battery Voltage Sensor

5.9 RF transmitter

There are two parts that build up the RF transmitter: RF encode generator and PLL/PA(PLL and RF output power amplifier). The RF encode generator receives parallel data from the CPU and encode them with the selected encoding format and shift the data bits to the PLL/PA. PLL/PA turn on/off the PLL/PA control signals at specified time according to the serial data received from the RF encode generator.

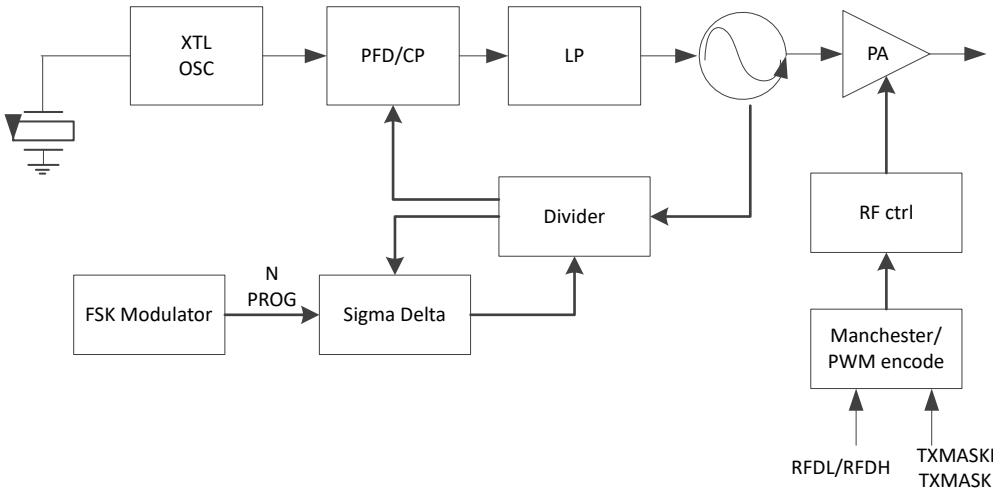


Figure 5-6 RF1 transmitter block

5.9.1 Manchester/PWM Encoder

The bit stream is usually encoded in an appropriate encoding scheme (e.g. Manchester, PWM, etc) for better data recovery. The chip supports Mark Space, Manchester and PWM encoding format.

The encode format is determined by the following register bits:

Table 5-7 Encode format configuration table

SYSCON3[0]	SYSCON3 [1]	SYSCON3 [2]	Encode format
1	0	x	Mark Space
0	0	0	Manchester
0	0	1	PWM

SYSCON3[0]	SYSCON3 [1]	SYSCON3 [2]	Encode format
0	1	0	Bi-Phase0
0	1	1	Bi-Phase1
1	1	0	DBi-Phase0
1	1	1	DBi-Phase1

The following is RF encoder output for the different formats:

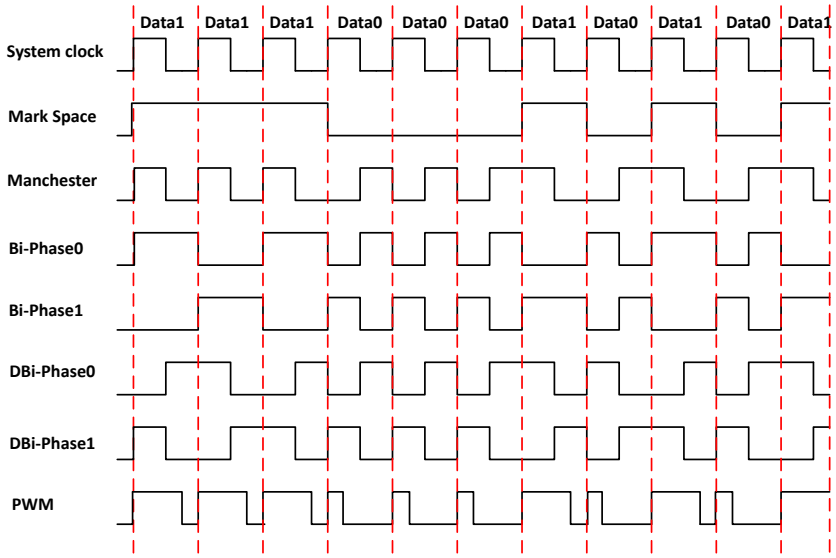


Figure 5-7 RF encoder

5.9.2 SD-PLL

There is a fractional-N PLL and can provide 315MHz and 433.92MHz output from 24MHz crystal or 12MHz as a backup option. Following the output of PLL, an internal PA is implemented to the external antenna through a matching circuit.

In ASK mode, the PLLFREQ0L/ PLLFREQ0H determines the carrier frequency.

In FSK mode, bit data 0 frequency is determined by the 13-bit value in the PLLFREQ0H/PLLFREQ0L and bit data 1 frequency by the 13-bit value in the PLLFREQ1H/ PLLFREQ1L.

These registers must be set prior to data transmissions and ideally should be set before PLL tuning.

$$f_{PLL} = f_{PLL\_REF} \times (N + \frac{PROG}{2^{13}})$$

Where f_{PLL_REF} is the PLL reference clock(12MHz), PROG is the value of PLLFREQ0H/ PLLFREQ0L or PLLFREQ1H/PLLFREQ1L, N is fixed and it depends on the value of PLL_F433_EN (RFCON1H[7]).

The frequency limits of PLL are as following:

Table 5-8 PLL frequency output of FSK modulation 24MHz

PLL_F433_EN(RFCON1H [7])	N	PROG1(decimal)	PROG1(heximal)	Frequency of PLL (MHz)
0	26	0	0	312
0	26	2048	0x800	315

PLL_F433_EN(RFCON1H [7])	N	PROG1(decimal)	PROG1(heximal)	Frequency of PLL (MHz)
0	26	8192	0x2000	323.9985
1	36	0	0	432
1	36	1310	0x51E	433.92
1	36	8192	0x2000	443.9985

5.9.3 FSK Modulator

The FSK modulator is part of the SD-PLL. The SD modulator generates a data stream that corresponds to the FSK low frequency if the FSK data line is low and a data stream that corresponds to the FSK high frequency if the data line is high.FSK high frequency and FSK low frequency are determined by an 13-bit value PROG.

$$f_{FSK\_HIGH} = f_{PLL\_REF} \times (N + \frac{PLLREQ1}{2^{13}})$$

$$f_{FSK\_LOW} = f_{PLL\_REF} \times (N + \frac{PLLREQ0}{2^{13}})$$

5.9.4 ASK Modulator

ASK center frequency is determined by an 13-bit value PROG.

$$f_{ASK\_CENRER} = f_{PLL\_REF} \times (N + \frac{PLLREQ0}{2^{13}})$$

5.9.5 RF Power Amplifier

In ASK mode, the PA toggles in sympathy with the serial transmission data. In FSK mode, the PA is active after the PLL is enabled and settles and remain active for the entire duration of the transmission.

The PA is automatically muted if the PLL lost lock duration transmission. In this situation, the PLL_LOCK_ALARM interrupt is asserted to indicate this fault.

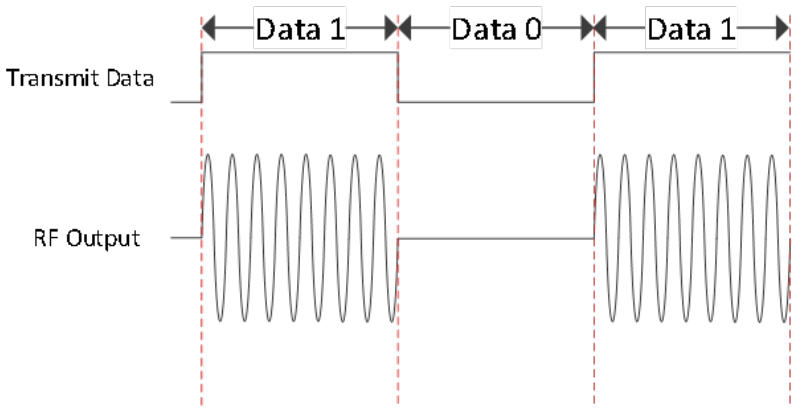


Figure 5-8 ASK modulation

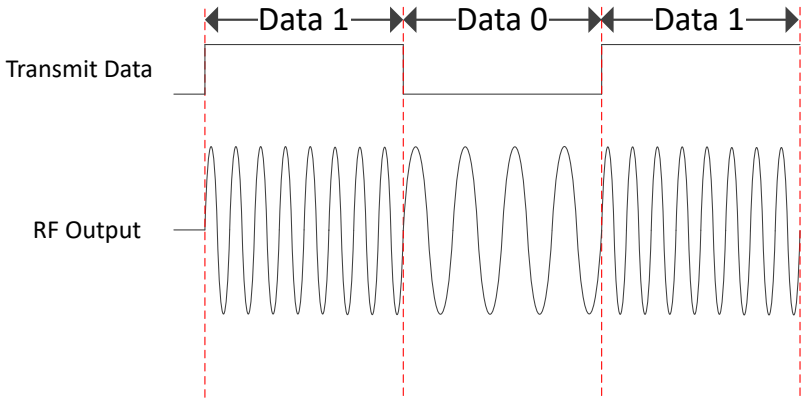


Figure 5-9 FSK modulation

5.9.6 Crystal Oscillator

The SNP73X has a Pierce oscillator for generating the reference frequency for RF transmission. And the 26MHz, 16MHz, 24MHz crystal oscillator can be selectable.

5.9.7 RF Baud-Rate Generator

The baud rate setting is determined by the following register bits:

Table 5-9 RF TX baud rate configuration

SYSCON3 [7]	SYSCON3[6]	Timing Rate of Baud Rate for MarkSpace/Manchester	Timing Rate of Baud Rate for PWM
0	0	1/4	1/6
0	1	1/16	1/24
1	0	1/8	1/12
1	1	1/2	1/3

$$BaudRate = TimingRate \times f_{SYS\_CLK}$$

5.10 RF Transmission Controller

The RF transmission controller is a state machine (FSM) for handling RF transmission without CPU support. The payload of the RF telegram needs to be generated in application code and stored in the upper RAM bank, starting at address 0x80. Then the RF transmission controller will be enabled and the device will be switched into system idle state for power saving. The CPU is halted/paused, while the RF state machine directly accesses to the RAM, and automatically transfers the data bytes of the payload to the manchester/ PWM encoder. The RF transmission controller also carries out the power management for RF transmission by controlling the PLL circuit, the crystal oscillator and the encoder.

The user can use the firmware function SendRfFrameXtal() to configure the RF transmission.

5.11 LF Receiver

The LF is designed for a carrier frequency of 125 kHz and for receiving manchester encoded data telegrams with a typical baud rate of 3900 bit/s. It is used for wake-up from power-down either by carrier detection (carrier wave detection mode) or telegram pattern match (telegram reception mode) for the following reasons:

- Triggering a pressure and temperature measurement;
- Triggering the transmission of a unique ID number;
- Triggering of operation modes;
- Update of user configuration data or user's applications.

5.11.1 LF Analog Front End (AFE)

The coil signal is amplified with an AGC and two cascade amplifiers and comparator. The data is decoded and captured. This mode support manchester format frame.

This LF system minimizes power consumption by allowing flexibility in choosing the ratio of on to off times (LF_LP_OFFCNTH, LF_LP_OFFCNTL, LF_LP_ONCNT) and by turning off power to blocks of circuitry until they are needed during signal reception and protocol recognition. In addition, this LF system can autonomously listen to valid LF signals, check for protocol and ID information which defined by wakeup pattern (LFWAKEH, LFWAKEL), and open the LF wakeup POWERDOWN flag enable bit PCON[4](LF_WAKE_EN), hardware will check pattern match automatically , then decide whether to open MCU power domain. So, the MCU can remain in a very low power mode until valid message has been detected.

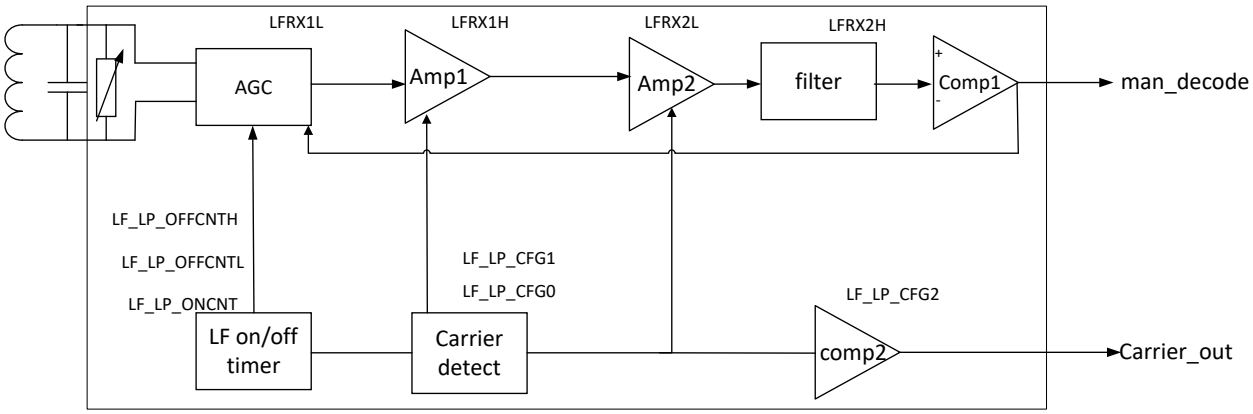


Figure 5-10 AFE

5.11.2 LF Digital Baseband (DBB)

The LF can be configured for various message protocols and telegrams to allow it to be used in a broad range of applications. Block FSM and counter will use analog part signal “man_decode” to refer and judge whether valid LF message is received. SFR LFWORDCNT can config max multiply of16 bits data.

The message preamble must be a series of Manchester coded bits at the nominal 3.906-kbps (Tbit) data rate. A synchronization pattern is used to mark the boundary between the preamble and the beginning of Manchester encoded information in the message body.

The synchronization pattern is a non-Manchester specific pattern. Only if valid synchronization pattern is received, the LF will receive data messages, the data messages can include a 16-bit WAKEID value and other more bytes data. Messages may contain any number of data bytes, block ser2par will storage the data, user can read from LFRXDH and LFRXDL when SFR INTL[5] (LFINT_ON) is set to 1 by hardware automatically, max word data number(including WAKEID) is defined by SFR LFWORDCNT. with the end-of-message indicated by detecting an illegal Manchester bit at a data byte boundary.

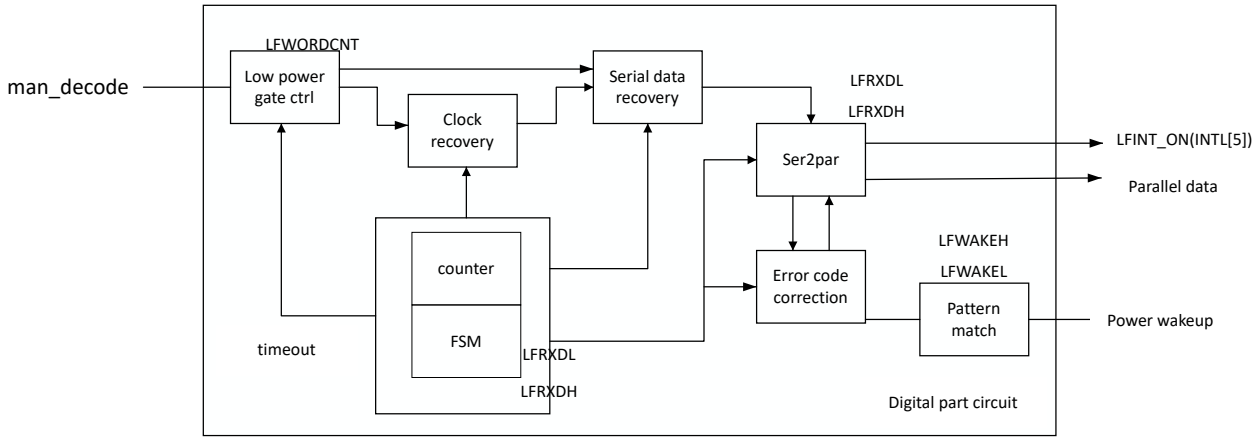


Figure 5-11 LF digital baseband block diagram

5.11.3 LF telegram

LF telegrams must start with a preamble in order to let the receiver establish an appropriate threshold for data demodulation. Preamble length must match LF Data Threshold settling time. It is followed by a defined synchronization pattern. Following the sync pattern comes a 16-bit long wake-up ID and an arbitrary number of data bytes. Wake-up ID and data bytes are Manchester encoded.

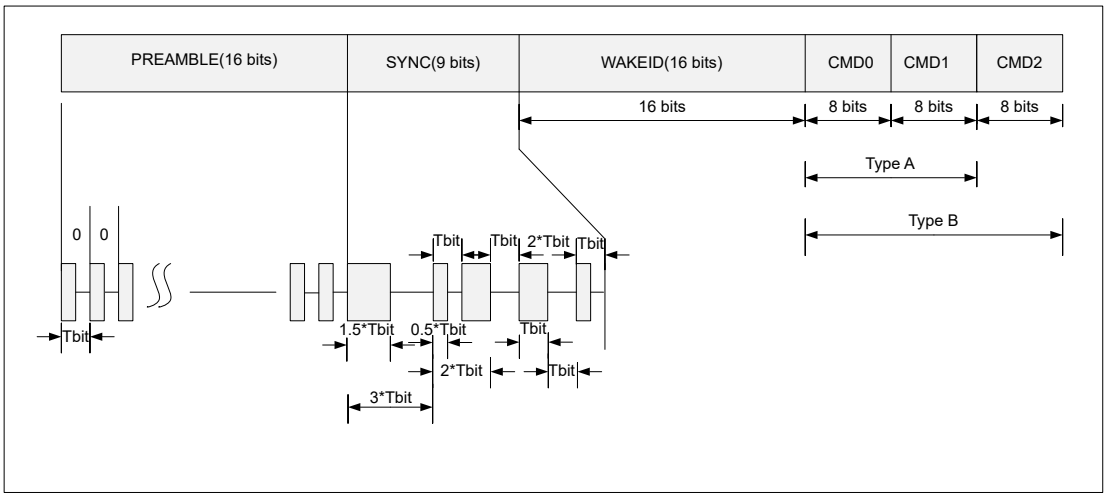


Figure 5-12 LF telegram

5.11.4 LF state machine

Associated firmware functions:

- LIB_LF_MSG_RX()
- LIB_CD_MSG_RX()

5.12 I/O-Port

The SNP739D features 6 general purpose I/O ports that can be accessed in application code via SFR.

When the device is powered on, it reads the GPIO1~0 input level status. If the status is' 01 ', it will enter the debugging mode; if the status is' 10', it will enter the programming mode, otherwise it will enter the normal mode.

All the GPIO can be configured for device wake-up from Powerdown state or resume from Idle state by an external digital signal.

If the hardware IIC is enabled GPIO0 is used for the SCL signal and GPIO1 for the SDA signal;

If the hardware UART is enabled GPIO3 is used for the TX signal and GPIO4 for the RX signal;

If the hardware SPI is enabled GPIO2 is used for the SSN signal, GPIO3 for the MOSI signal, GPIO4 for the MISO signal, and GPIO5 for the SCLK signal;

If the PWM of timer8 is enabled GPIO2 is used for PWM CH0 output, GPIO4 for PWM CH1 output.

Each GPIO has pull-up and pull-down resistor. In Powerdown state and Thermal shutdown state the GPIOs keep their configuration.

Table 5-10 GPIOs function definition

PIN	Function	I/O	Description
GPIO0	I2C SCL	I	I2C serial clock line. Configured to I2C clock pin if I2CEN is set. Weak-high has to be provide either by the internal pullup resistor,or by I2C master at external.
	Port pin I/O	I/O	General purpose IO
GPIO1	I2C SDA	I/O	I2C serial data. Configured to I2C clock pin if I2CEN is set. Weak-high has to be provide either by the internal pullup resistor,or by I2C master at external.
	Port pin I/O	I/O	General purpose IO
GPIO2	RF TX data	I	RF encoder data output If RFTXEN is set,the Manchester/Bi-phase encode is delivered serially to GPIO2
	Port pin I/O	I/O	General purpose IO
	PWM CH0 OUTPUT	O	PWM channel 0 output
	SPI SSN	I/O	Slave select (ssn) input for SPI non-dma mode. Slave select (ssn) output for SPI master dma mode.

PIN	Function	I/O	Description
GPIO3	SPI MOSI	I/O	Master data output or Slave data input for SPI
	UART/LIN TXD	O	Transmit data output for UART
	Port pin I/O	I/O	General purpose IO
	TEST signal output	O	Test0 signal output
GPIO4	SPI MISO	I/O	Master data input or Slave data output for SPI
	UART/LIN RXD	I/O	Receive data input for UART or Receive clock output for UART mode0
	Port pin I/O	I/O	General purpose IO
	PWM CH1 OUTPUT	O	PWM channel 1 output
	TEST signal output	O	Test1 signal output
GPIO5	SPI SCLK	I/O	Master clock output or Slave clock input for SPI
	Port pin I/O	I/O	General purpose IO
	EXCLK	I	External Clock input for system clock

Associated registers:

- GPIODAT
- GPIODATN
- GPIODIR
- GPIOPUPD

6 Application Circuit

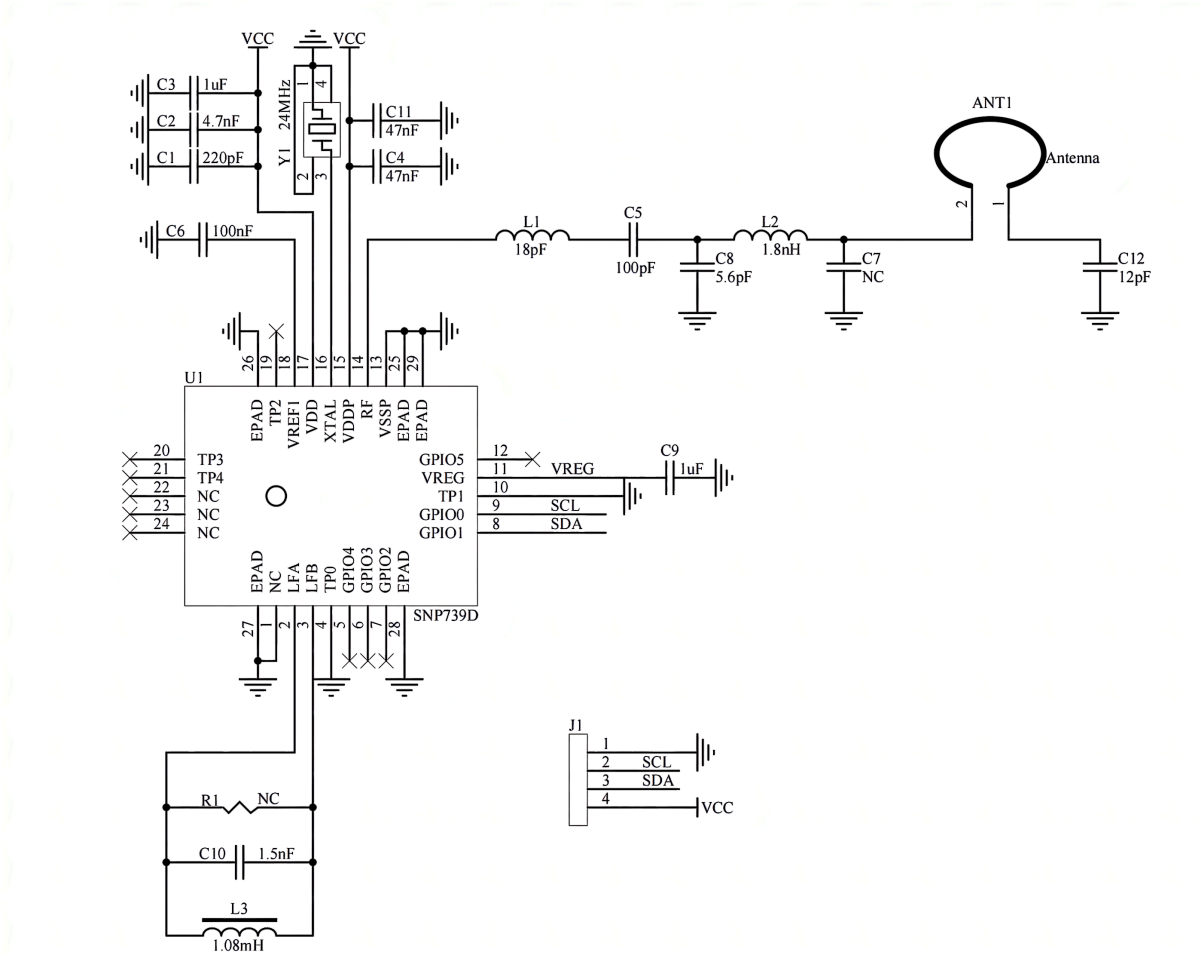
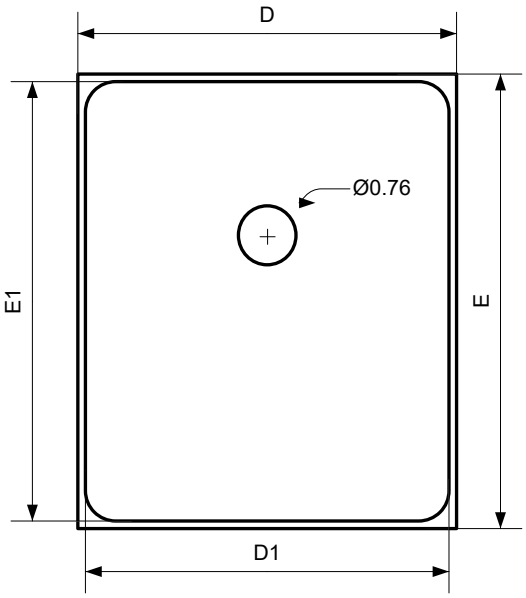


Figure 6-1 Application Circuit

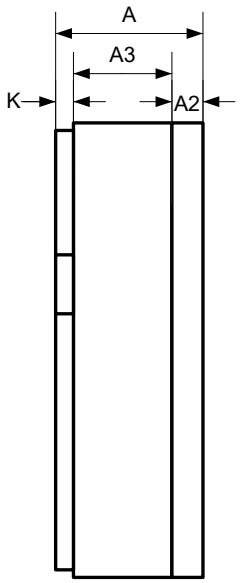
Note: L1/C5/C8/L2/C7/C12 value might be changed according to different antenna.

7 Package Information

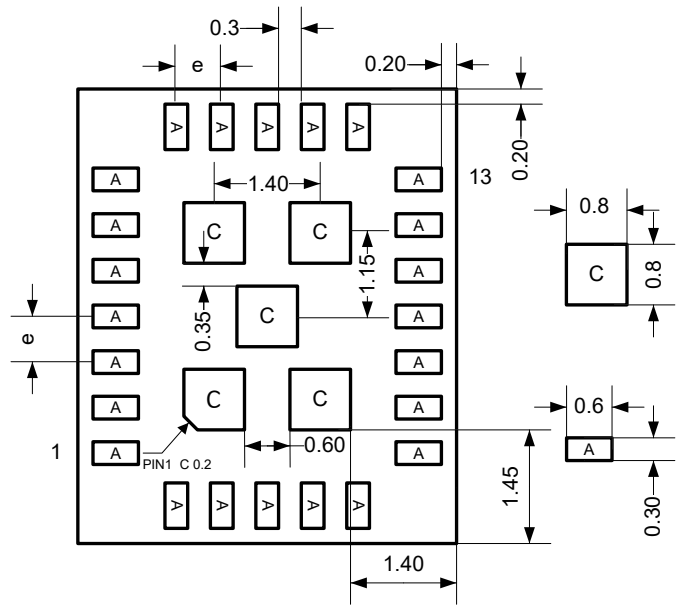
7.1 Package Outline



TOP VIEW



SIDE VIEW



BOTTOM VIEW

MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	1.75	1.85	1.95
A2	0.27	0.32	0.37
A3	1.33	1.38	1.43
K	0.12	0.15	0.18
D	4.90	5.00	5.10
D1	4.80	4.85	4.90
E	5.90	6.00	6.10
E1	5.80	5.85	5.90
e	BSC 0.6		

Figure 7-1 Package Outline

7.2 Footprint

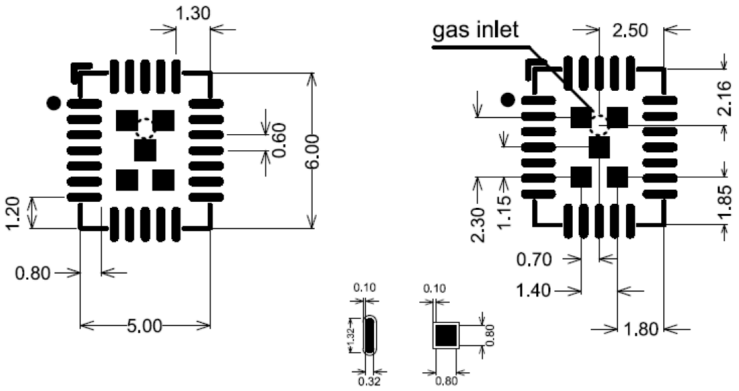


Figure 7-2 Recommend footprint layout

7.3 Marking

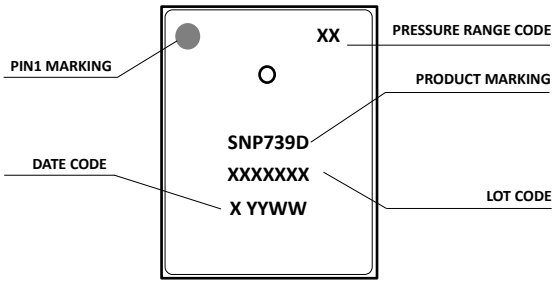


Figure 7-3 Marking information

Note:
1.DATE CODE, the first X is 3, 3 representing 900kPa, YY representing year (When YY are “22”, means 2022), WW representing week (When WW are “09”, means the 9th week of the year).
2.Pressure range CODE, 51 representing 900kPa.

8 Revision History

Table 8-1 Revision History

VERSION	DATE	NOTE
1.0	2020/12/09	Initial version
1.1	2021/10/22	Modify temperature accuracy; add order information
1.2	2021/11/11	Modify marking information
1.3	2022/02/15	Modify standby current; Modify Table 3-1 Absolute Maximum Ratings; Modify Table 3-2 Operating Range; Fixed Pin information error in Figure10-1 Block Diagram; Fixed Pin information error in Figure7-2 Application Circuit.
1.4	2022/02/25	Pin 1: Connect to GND.
1.5	2022/3/7	Modify application circuit.
1.6	2022/5/5	Modify Table 4-16 RF Transmitter Characteristics, Figure7-1 Application Circuit, Figure 8-1 Package Dimension, Figure 8-3 Marking information.
1.7	2022/6/16	Modify Figure 5-2 Power-On and Under-Voltage Reset Behavior.
1.8	2022/9/26	Delete 0ptional 8-bit long wake-up ID in chapter 5.12.3 LF telegram . Pin 4,Pin 10: Connect to GND. Modify Figure 6-1 Application Circuit.
1.9	2022/12/30	Modify order information and marking information.
2.0	2023/01/10	Modify order information.
2.1	2023/06/07	Delete model: SNP739D52CLE (measurement range:1900kPa).